

About PICMG 1.3

PICMG 1.3 (SHB Express™) Overview

As a solution, PICMG organization started development of new standard in last year that adopts PCI Express as external expansion.

- PICMG 1.3, so called "SHB Express" takes component side as ISA card that means it is the same as PICMG 1.0. Such setting makes signal routing among processor, memory controller hub and memory is more smoothly and it can leverage chassis design for PICMG 1.0.
- Same as PICMG 1.2 (ePCI-X), SHB Express defined both full-size and half-size SHB.
- Slot for full-size SHB is combination of dual PCI Express x16 (Connector A & C) and dual PCI Express x8 slots (Connector B & D); one PCI Express x16 (Connector A) and one PCI Express x8 (Connector B) for half-size SHB. Therefore, this new standard does not compatible with either PICMG 1.0 or 1.2.
- Electrical Function of edge connectors:
 - Connect A & B: PCI Express Link; configuration could be one x16 or two x8 or one x8 and two x4 or four x4
 - Connect C & B: Additional power and I/O
 - Connect D: One 32-bit PCI(-X) bus
- More +12V power input pins are defined in PICMG 1.3 because new Intel Pentium 4 processor consumes more than 100W and the efficiency is lower for utilized +5V transformation. By the way, 20A up current leads transformation circuit generating more heat; therefore, life-time of the SHB will decrease accordingly.
- Insertion loss of serial type signals are also limited in the specification due to the edge connectors is break point of impedance, therefore, serial type signal has reflection and attenuation issues.
- Miscellaneous I/O ports such as USB, SATA and Gigabit Ethernet can be routed to backplane that features more reliable signal quality and minimum length of cables.
- IPMB (Intelligent Platform Management Bus) and SMBus are also reserved for connection of system management possibility

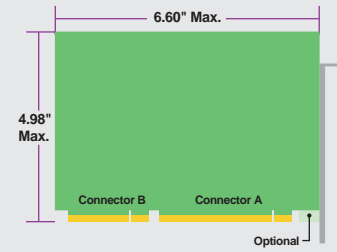


Figure 5: Dimension drawing of half-size SHB

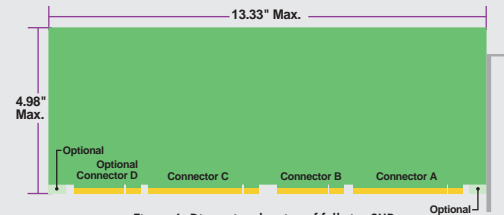


Figure 6: Dimension drawing of full-size SHB

Table: PCIe Link Configurations

Configuration	A0 (x16)				Ref Clks for all Ports (up to 8 Clks)	A0 (x4)			
	A2 (x8)		A0 (x8)			B3 (x1)	B2 (x1)	B1 (x1)	B0 (x1)
	A3 (x4)	A2 (x4)	A1 (x4)	A0 (x4)					
c1	x16				(Ref Clks)	x4			
c2	second x8		first x8		(Ref Clks)	x4			
c3	third x4	second x4	x8		(Ref Clks)	first x4			
c4	fifth x4	fourth x4	third x4	second x4	(Ref Clks)	first x4			

A backplane should plumb the PCIe in the following order to maximize interoperability:

c5	8th	7th	6th	5th	4th	3rd	2nd	1st
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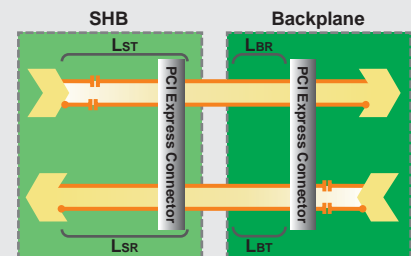


Figure 8: PCIe Insertion loss

Backplane Features

Off course, higher I/O bandwidth is introduced by this new form factor. Take, for example, applications like flight simulation, gaming, medical are need high performance graphics engine. In past, both PICMG 1.0 & 1.2 are not support AGP port on backplane. So, the only solution is having the graphics controller on-board. However, space and thermal constrain the power of graphics engine. For these applications, PICMG 1.3 is the solution that allows system to include latest and mighty graphics add-in card with PCI Express x16 interface.

PCI Express x16 graphics card utilization is just one merit of SHB Express standard. More than that, versatile backplane could fulfill your special requirement immediately. With native expansion interfaces that support by SHB, switch or bridge can be design-in to have more PCI Express slots or different kind of expansion bus such as PCI-X and PCI.

