COM Express Carrier Design Guide

Carrier design guideline for

PCOM-B700G-NS

Rev. 1.0

Revision history

Rev.	Date	Note
R1.0	2022/03	1st Release

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1 Introduction

The Carrier Design Guide provides the guideline of designing your own carrier board based on Portwell's COM Express Modular product PCOM-B700G-NS. PCOM-B B700G-NS is Type 7, 125x95mm Modular board, more information is included in PCOM-B700G-NS User's Guide and can be downloaded from Portwell download center (Or contact your Portwell sales representative for acquiring PCOM-B700G-NS User's Guide). This carrier design guide is dedicated for the designers designing a COM Express Type 7 carrier board which will have a excellent compatibility with Portwell's PCOM-B700G-NS modular product.

The layout guideline provided are 8 PCB layer stack up, each interface has three sections, which are detail PCOM-B700G-NS pin out, pin name, power rail, PU/PD, AC couple capacitor and etc. information are included. Second part contains PCB layout guide, impedance, maximum trace, trace width, and trace spacing etc. Third section provides the available trace length of which designers are able to optimize the high speed signals such as PCIE, SATA, USB etc.

2 PCOM-B700G-NS

2.1 PCOM-B700G-NS Block Diagram

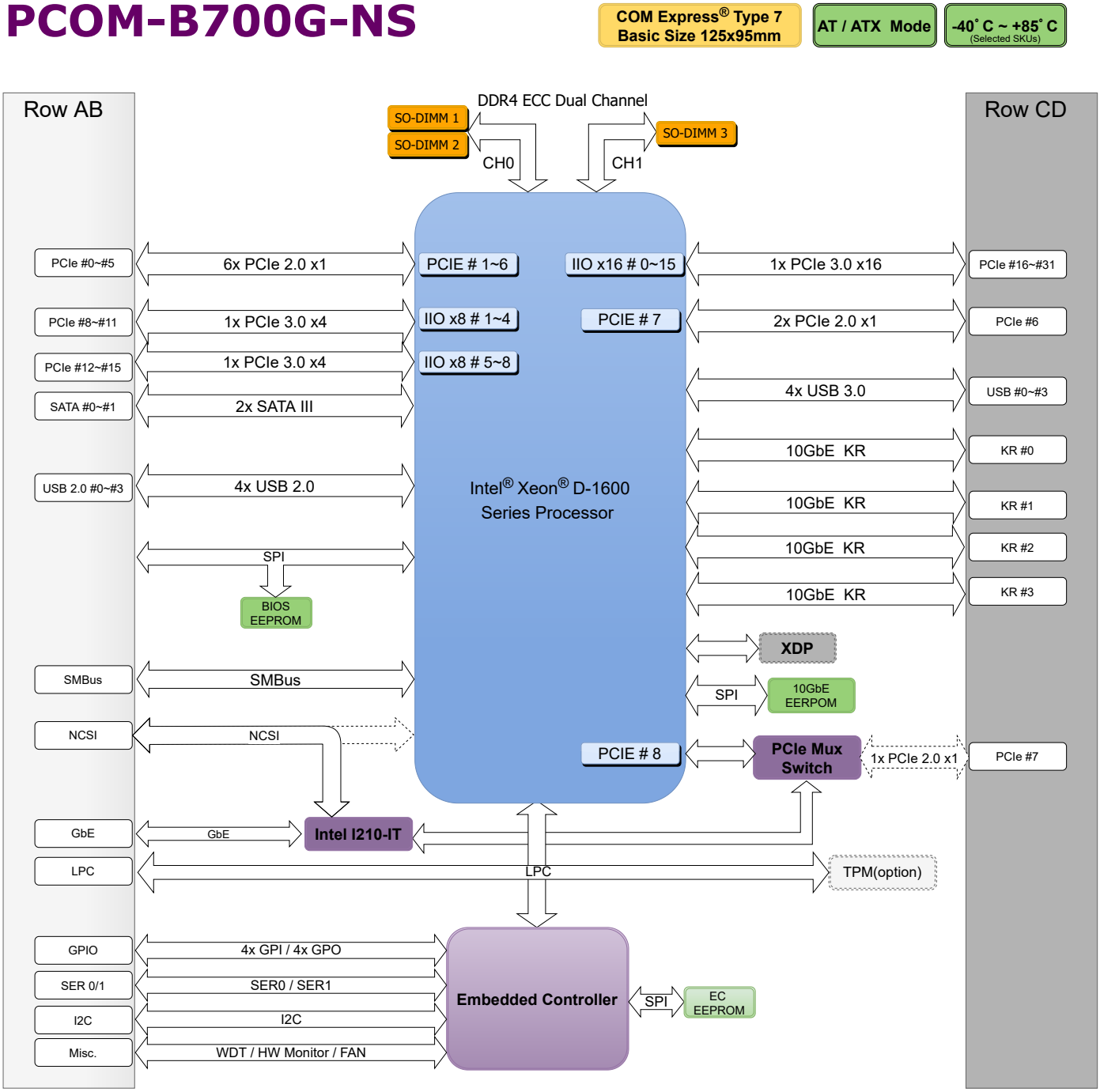


Figure 1 PCOM-B700G-NS Block Diagram

2.2 PCOM-B700G-NS Pin-out

PCOM-B700G-NS Type7 Pin-Out							
Pin	Row A	Pin	Row B	Pin	Row C	Pin	Row D
A1	GND(FIXED)	B1	GND(FIXED)	C1	GND(FIXED)	D1	GND(FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	GND	D2	GND
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	USB_SSRX0-	D3	USB_SSTX0-
A4	GBE0_LINK100#	B4	LPC_AD0	C4	USB_SSRX0+	D4	USB_SSTX0+
A5	GBE0_LINK1000#	B5	LPC_AD1	C5	GND	D5	GND
A6	GBE0_MDI2-	B6	LPC_AD2	C6	USB_SSRX1-	D6	USB_SSTX1-
A7	GBE0_MDI2+	B7	LPC_AD3	C7	USB_SSRX1+	D7	USB_SSTX1+
A8	GBE0_LINK#	B8	LPC_DRQ0#	C8	GND	D8	GND
A9	GBE0_MDI1-	B9	LPC_DRQ1#	C9	USB_SSRX2-	D9	USB_SSTX2-
A10	GBE0_MDI1+	B10	LPC_CLK	C10	USB_SSRX2+	D10	USB_SSTX2+
A11	GND(FIXED)	B11	GND(FIXED)	C11	GND(FIXED)	D11	GND(FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	USB_SSRX3-	D12	USB_SSTX3-
A13	GBE0_MDI0+	B13	SMB_CK	C13	USB_SSRX3+	D13	USB_SSTX3+
A14	NC	B14	SMB_DAT	C14	GND	D14	GND
A15	SUS_S3#	B15	SMB_ALERT#	C15	10G_PHY_MDC_SCL3	D15	10G_PHY_MDIO_SDA3
A16	SATA0_TX+	B16	SATA1_TX+	C16	10G_PHY_MDC_SCL2	D16	10G_PHY_MDIO_SDA2
A17	SATA0_TX-	B17	SATA1_TX-	C17	10G_SDP2	D17	10G_SDP3
A18	SUS_S4#	B18	SUS_STAT#	C18	GND	D18	GND
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCIE_RX6+	D19	PCIE_TX6+
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCIE_RX6-	D20	PCIE_TX6-
A21	GND(FIXED)	B21	GND(FIXED)	C21	GND(FIXED)	D21	GND(FIXED)
A22	PCIE_TX15+	B22	PCIE_RX15+	C22	PCIE_RX7+	D22	PCIE_TX7+
A23	PCIE_TX15-	B23	PCIE_RX15-	C23	PCIE_RX7-	D23	PCIE_TX7-
A24	SUS_S5#	B24	PWR_OK	C24	10G_INT2	D24	10G_INT3
A25	PCIE_TX14+	B25	PCIE_RX14+	C25	GND	D25	GND
A26	PCIE_TX14-	B26	PCIE_RX14-	C26	10G_KR_RX3+	D26	10G_KR_TX3+
A27	BATLOW#	B27	WDT	C27	10G_KR_RX3-	D27	10G_KR_TX3-
A28	(S)ATA_ACT#	B28	NC	C28	GND	D28	GND
A29	NC	B29	NC	C29	10G_KR_RX2+	D29	10G_KR_TX2+
A30	NC	B30	NC	C30	10G_KR_RX2-	D30	10G_KR_TX2-

A31	GND(FIXED)	B31	GND(FIXED)	C31	GND(FIXED)	D31	GND(FIXED)
A32	NC	B32	SPKR	C32	10G_SFP_SDA3	D32	10G_SFP_SCL3
A33	NC	B33	I2C_CK	C33	10G_SFP_SDA2	D33	10G_SFP_SCL2
A34	BIOS_DIS0#	B34	I2C_DAT	C34	10G_PHY_RST_23	D34	10G_PHY_CAP_23
A35	THRMTRIP#	B35	THRM#	C35	10G_PHY_RST_01	D35	10G_PHY_CAP_01
A36	PCIE_TX13+	B36	PCIE_RX13+	C36	10G_LED_SDA	D36	NC
A37	PCIE_TX13-	B37	PCIE_RX13-	C37	10G_LED_SCL	D37	NC
A38	GND	B38	GND	C38	10G_SFP_SDA1	D38	10G_SFP_SCL1
A39	PCIE_TX12+	B39	PCIE_RX12+	C39	10G_SFP_SDA0	D39	10G_SFP_SCL0
A40	PCIE_TX12-	B40	PCIE_RX12-	C40	10G_SDP0	D40	10G_SDP1
A41	GND(FIXED)	B41	GND(FIXED)	C41	GND(FIXED)	D41	GND(FIXED)
A42	USB2-	B42	USB3-	C42	10G_KR_RX1+	D42	10G_KR_TX1+
A43	USB2+	B43	USB3+	C43	10G_KR_RX1-	D43	10G_KR_TX1-
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	GND	D44	GND
A45	USB0-	B45	USB1-	C45	10G_PHY_MDC_SCL1	D45	10G_PHY_MDIO_SDA1
A46	USB0+	B46	USB1+	C46	10G_PHY_MDC_SCL0	D46	10G_PHY_MDIO_SDA0
A47	VCC_RTC	B47	NC	C47	10G_INT0	D47	10G_INT1
A48	NC	B48	NC	C48	GND	D48	GND
A49	GBE0_SDP	B49	SYS_RESET#	C49	10G_KR_RX0+	D49	10G_KR_TX0+
A50	LPC_SERIRQ	B50	CB_RESET#	C50	10G_KR_RX0-	D50	10G_KR_TX0-
A51	GND(FIXED)	B51	GND(FIXED)	C51	GND(FIXED)	D51	GND(FIXED)
A52	PCIE_TX5+	B52	PCIE_RX5+	C52	PCIE_RX16+	D52	PCIE_TX16+
A53	PCIE_TX5-	B53	PCIE_RX5-	C53	PCIE_RX16-	D53	PCIE_TX16-
A54	GPI0	B54	GPO1	C54	TYPE0#	D54	NC
A55	PCIE_TX4+	B55	PCIE_RX4+	C55	PCIE_RX17+	D55	PCIE_TX17+
A56	PCIE_TX4-	B56	PCIE_RX4-	C56	PCIE_RX17-	D56	PCIE_TX17-
A57	GND	B57	GPO2	C57	TYPE1#	D57	TYPE2#
A58	PCIE_TX3+	B58	PCIE_RX3+	C58	PCIE_RX18+	D58	PCIE_TX18+
A59	PCIE_TX3-	B59	PCIE_RX3-	C59	PCIE_RX18-	D59	PCIE_TX18-
A60	GND(FIXED)	B60	GND(FIXED)	C60	GND(FIXED)	D60	GND(FIXED)

A61	PCIE_TX2+	B61	PCIE_RX2+	C61	PCIE_RX19+	D61	PCIE_TX19+
A62	PCIE_TX2-	B62	PCIE_RX2-	C62	PCIE_RX19-	D62	PCIE_TX19-
A63	GPI1	B63	GPO3	C63	NC	D63	NC
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	NC	D64	NC
A65	PCIE_TX1-	B65	PCIE_RX1-	C65	PCIE_RX20+	D65	PCIE_TX20+
A66	GND	B66	WAKE0#	C66	PCIE_RX20-	D66	PCIE_TX20-
A67	GPI2	B67	WAKE1#	C67	RAPID_SHUTDOWN	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68	PCIE_RX21+	D68	PCIE_TX21+
A69	PCIE_TX0-	B69	PCIE_RX0-	C69	PCIE_RX21-	D69	PCIE_TX21-
A70	GND(FIXED)	B70	GND(FIXED)	C70	GND(FIXED)	D70	GND(FIXED)
A71	PCIE_TX8+	B71	PCIE_RX8+	C71	PCIE_RX22+	D71	PCIE_TX22+
A72	PCIE_TX8-	B72	PCIE_RX8-	C72	PCIE_RX22-	D72	PCIE_TX22-
A73	GND	B73	GND	C73	GND	D73	GND
A74	PCIE_TX9+	B74	PCIE_RX9+	C74	PCIE_RX23+	D74	PCIE_TX23+
A75	PCIE_TX9-	B75	PCIE_RX9-	C75	PCIE_RX23-	D75	PCIE_TX23-
A76	GND	B76	GND	C76	GND	D76	GND
A77	PCIE_TX10+	B77	PCIE_RX10+	C77	NC	D77	NC
A78	PCIE_TX10-	B78	PCIE_RX10-	C78	PCIE_RX24+	D78	PCIE_TX24+
A79	GND	B79	GND	C79	PCIE_RX24-	D79	PCIE_TX24-
A80	GND(FIXED)	B80	GND(FIXED)	C80	GND(FIXED)	D80	GND(FIXED)
A81	PCIE_TX11+	B81	PCIE_RX11+	C81	PCIE_RX25+	D81	PCIE_TX25+
A82	PCIE_TX11-	B82	PCIE_RX11-	C82	PCIE_RX25-	D82	PCIE_TX25-
A83	GND	B83	GND	C83	NC	D83	NC
A84	NCSI_TX_EN	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85	PCIE_RX26+	D85	PCIE_TX26+
A86	NC	B86	VCC_5V_SBY	C86	PCIE_RX26-	D86	PCIE_TX26-
A87	NC	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	PCIE_CK_REF+	B88	BIOS_DIS1#	C88	PCIE_RX27+	D88	PCIE_TX27+
A89	PCIE_CK_REF-	B89	NC	C89	PCIE_RX27-	D89	PCIE_TX27-
A90	GND(FIXED)	B90	GND(FIXED)	C90	GND(FIXED)	D90	GND(FIXED)

A91	SPI_POWER	B91	NCSI_CLK_IN	C91	PCIE_RX28+	D91	PCIE_TX28+
A92	SPI_MISO	B92	NCSI_RXD1	C92	PCIE_RX28-	D92	PCIE_TX28-
A93	GPO0	B93	NCSI_RXD0	C93	GND	D93	GND
A94	SPI_CLK	B94	NCSI_CRS_DV	C94	PCIE_RX29+	D94	PCIE_TX29+
A95	SPI_MOSI	B95	NCSI_TXD1	C95	PCIE_RX29-	D95	PCIE_TX29-
A96	NC	B96	NCSI_TXD0	C96	GND	D96	GND
A97	TYPE10#	B97	SPI_CS#	C97	NC	D97	NC
A98	SER0_TX	B98	NCSI_ARB_IN	C98	PCIE_RX30+	D98	PCIE_TX30+
A99	SER0_RX	B99	NCSI_ARB_OUT	C99	PCIE_RX30-	D99	PCIE_TX30-
A100	GND(FIXED)	B100	GND(FIXED)	C100	GND(FIXED)	D100	GND(FIXED)
A101	SER1_TX	B101	FAN_PWMOUT	C101	PCIE_RX31+	D101	PCIE_TX31+
A102	SER1_RX	B102	FAN_TACHIN	C102	PCIE_RX31-	D102	PCIE_TX31-
A103	LID#	B103	SLEEP#	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND(FIXED)	B110	GND(FIXED)	C110	GND(FIXED)	D110	GND(FIXED)

Table 1 PCOM-B700G-NS Pin-Out

3 COM Express Interface

3.1 PCIe

PCOM-B700G-NS PCIe #0 ~ #31 Tx signal

Pin#	Pin Name	COMe 3.0 Specification (Signals Requiring Module Termination)	Pin Typ	B700G-NS Module	Pwr Rail / Tolerance(Volt)
A68	PCIE_TX0+	AC coupled on the Module	O PCIE	0.22uF AC coupled on the Module(Gen2).	AC coupled on Module
A69	PCIE_TX0-				
A64	PCIE_TX1+				
A65	PCIE_TX1-				
A61	PCIE_TX2+				
A62	PCIE_TX2-				
A58	PCIE_TX3+				
A59	PCIE_TX3-				
A55	PCIE_TX4+				
A56	PCIE_TX4-				
A52	PCIE_TX5+				
A53	PCIE_TX5-				
D19	PCIE_TX6+				
D20	PCIE_TX6-				
D22	PCIE_TX7+				
D23	PCIE_TX7-				
A71	PCIE_TX8+			0.22uF AC coupled on the Module(Gen3).	
A72	PCIE_TX8-				
A74	PCIE_TX9+				
A75	PCIE_TX9-				
A77	PCIE_TX10+				
A78	PCIE_TX10-				
A81	PCIE_TX11+				
A82	PCIE_TX11-				
A39	PCIE_TX12+				
A40	PCIE_TX12-				
A36	PCIE_TX13+				
A37	PCIE_TX13-				
A25	PCIE_TX14+				
A26	PCIE_TX14-				
A22	PCIE_TX15+				
A23	PCIE_TX15-				
D52	PCIE_TX16+				
D53	PCIE_TX16-				
D55	PCIE_TX17+				
D56	PCIE_TX17-				
D58	PCIE_TX18+				
D59	PCIE_TX18-				
D61	PCIE_TX19+				
D62	PCIE_TX19-				
D65	PCIE_TX20+				
D66	PCIE_TX20-				
D68	PCIE_TX21+				
D69	PCIE_TX21-				
D71	PCIE_TX22+				
D72	PCIE_TX22-				
D74	PCIE_TX23+				
D75	PCIE_TX23-				
D78	PCIE_TX24+				
D79	PCIE_TX24-				
D81	PCIE_TX25+				
D82	PCIE_TX25-				
D85	PCIE_TX26+				
D86	PCIE_TX26-				
D88	PCIE_TX27+				
D89	PCIE_TX27-				
D91	PCIE_TX28+				
D92	PCIE_TX28-				
D94	PCIE_TX29+				
D95	PCIE_TX29-				
D98	PCIE_TX30+				
D99	PCIE_TX30-				
D101	PCIE_TX31+				
D102	PCIE_TX31-				

Table 2 B700G-NS PCIE TX

PCOM-B700G-NS PCIe #0 ~ #31 Rx signal

Pin#	Pin Name	COMe 3.0 Specification (Signals Requiring Module Termination)	Pin Typ	B700G-NS Module	Pwr Rail / Tolerance(Volt)
B68	PCIE_RX0+	AC coupled off the Module.	I PCIE	AC coupled off Module	AC coupled off Module
B69	PCIE_RX0-				
B64	PCIE_RX1+				
B65	PCIE_RX1-				
B61	PCIE_RX2+				
B62	PCIE_RX2-				
B58	PCIE_RX3+				
B59	PCIE_RX3-				
B55	PCIE_RX4+				
B56	PCIE_RX4-				
B52	PCIE_RX5+				
B53	PCIE_RX5-				
C19	PCIE_RX6+				
C20	PCIE_RX6-				
C22	PCIE_RX7+				
C23	PCIE_RX7-				
B71	PCIE_RX8+				
B72	PCIE_RX8-				
B74	PCIE_RX9+				
B75	PCIE_RX9-				
B77	PCIE_RX10+				
B78	PCIE_RX10-				
B81	PCIE_RX11+				
B82	PCIE_RX11-				
B39	PCIE_RX12+				
B40	PCIE_RX12-				
B36	PCIE_RX13+				
B37	PCIE_RX13-				
B25	PCIE_RX14+				
B26	PCIE_RX14-				
B22	PCIE_RX15+				
B23	PCIE_RX15-				
C52	PCIE_RX16+				
C53	PCIE_RX16-				
C55	PCIE_RX17+				
C56	PCIE_RX17-				
C58	PCIE_RX18+				
C59	PCIE_RX18-				
C61	PCIE_RX19+				
C62	PCIE_RX19-				
C65	PCIE_RX20+				
C66	PCIE_RX20-				
C68	PCIE_RX21+				
C69	PCIE_RX21-				
C71	PCIE_RX22+				
C72	PCIE_RX22-				
C74	PCIE_RX23+				
C75	PCIE_RX23-				
C78	PCIE_RX24+				
C79	PCIE_RX24-				
C81	PCIE_RX25+				
C82	PCIE_RX25-				
C85	PCIE_RX26+				
C86	PCIE_RX26-				
C88	PCIE_RX27+				
C89	PCIE_RX27-				
C91	PCIE_RX28+				
C92	PCIE_RX28-				
C94	PCIE_RX29+				
C95	PCIE_RX29-				
C98	PCIE_RX30+				
C99	PCIE_RX30-				
C101	PCIE_RX31+				
C102	PCIE_RX31-				
A88	PCIE_CLK_REF+	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O PCIE	-	PCIE
A89	PCIE_CLK_REF-				

Table 3 B700G-NS PCIE RX

3.1.1 AC Coupling Capacitor

PCIE / PEG AC Coupling : Device Down

While PCIE devices are designed on COM Express Carrier Board, the AC coupling Capacitor should be added on the carrier, please refer to below diagram.

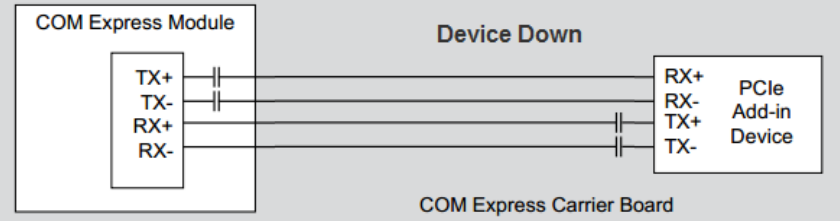


Figure 2 PCIE AC Coupling Capacitor - Device Down

(From PICMG COM Express Carrier Board Design Guide)

PCIE / PEG AC Coupling : Add-In Card

While PCIE devices are designed as Add In Card, the AC coupling Capacitor should be on PCIe Add-In Card, rather than on the COM Express Carrier Board, please refer to below diagram.

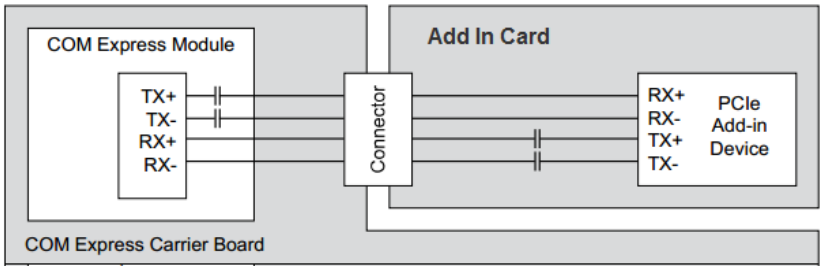


Figure 3 PCIE AC Coupling Capacitor - Add In Card

(From PICMG COM Express Carrier Board Design Guide)

3.1.2 PCB layout guideline - PCIe/PEG

Parameter	PCIe Gen1 / Gen2	PCIe Gen3
Bandwidth	2.5 G / 5 G	8 G
Maximum signal line length (coupled traces) TX and RX	12.0/10 inch	7/9 inch (Add In Card/ Device Down)
Differential impedance	85 Ω +/-12%	85 Ω +/-12%
Single-ended Impedance	50 Ω +/-12%	50 Ω +/-12%
Trace width (W)	4 mil PCB stack-up dependent	4 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	15 mil PCB stack-up dependent	15 mil PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 15mils	Min. 15mils
Length matching between differential pairs (intra-pair)	Max. 5mils	Max. 5mils
Reference plane	GND referenced preferred	GND referenced preferred
Spacing from edge of plane	Min. 10*W mils (W=trace width)	Min. 10*W mils (W=trace width)
Via Usage	Max. 4 vias per TX trace Max. 4 vias per RX trace	Max. 2 vias per TX trace Max. 2 vias per RX trace

Table 4 PCIE/PEG Layout information

3.1.3 Passive Devices

AC Cap value (Gen1/Gen2)	Min = 75nf Max = 265nf	PCOM-B700G-NS AC Cap value 220nF
AC Cap value (Gen3)	Min = 75nf Max = 265nf	

Table 5 PCIE/PEG AC coupling capacitor value

3.1.4 Reference schematic - PCOM-C701 ZR1

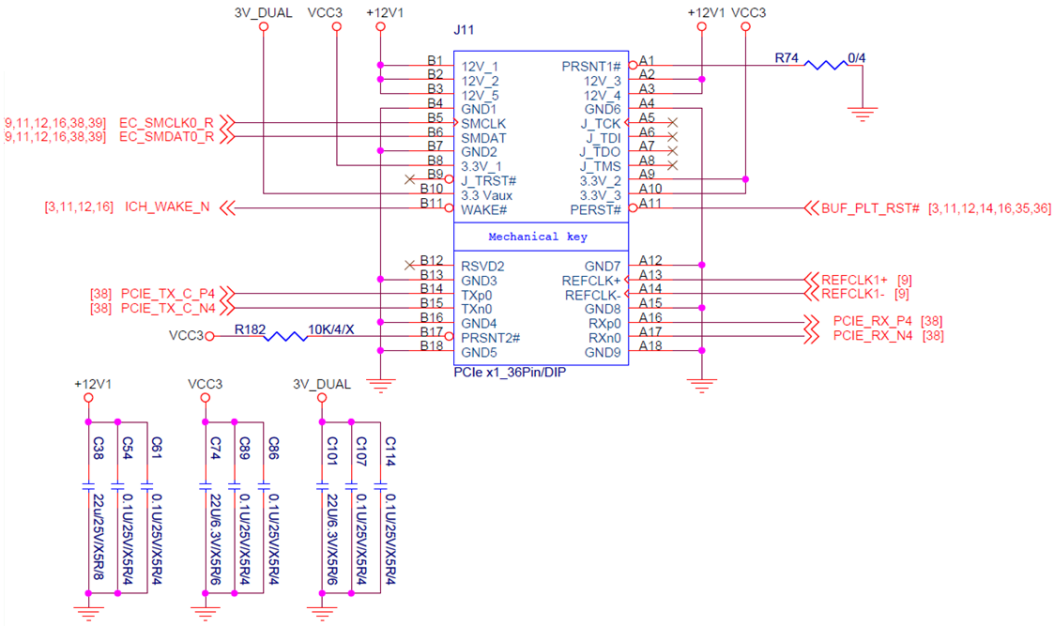


Figure 4 PCIEx1 reference schematic-1

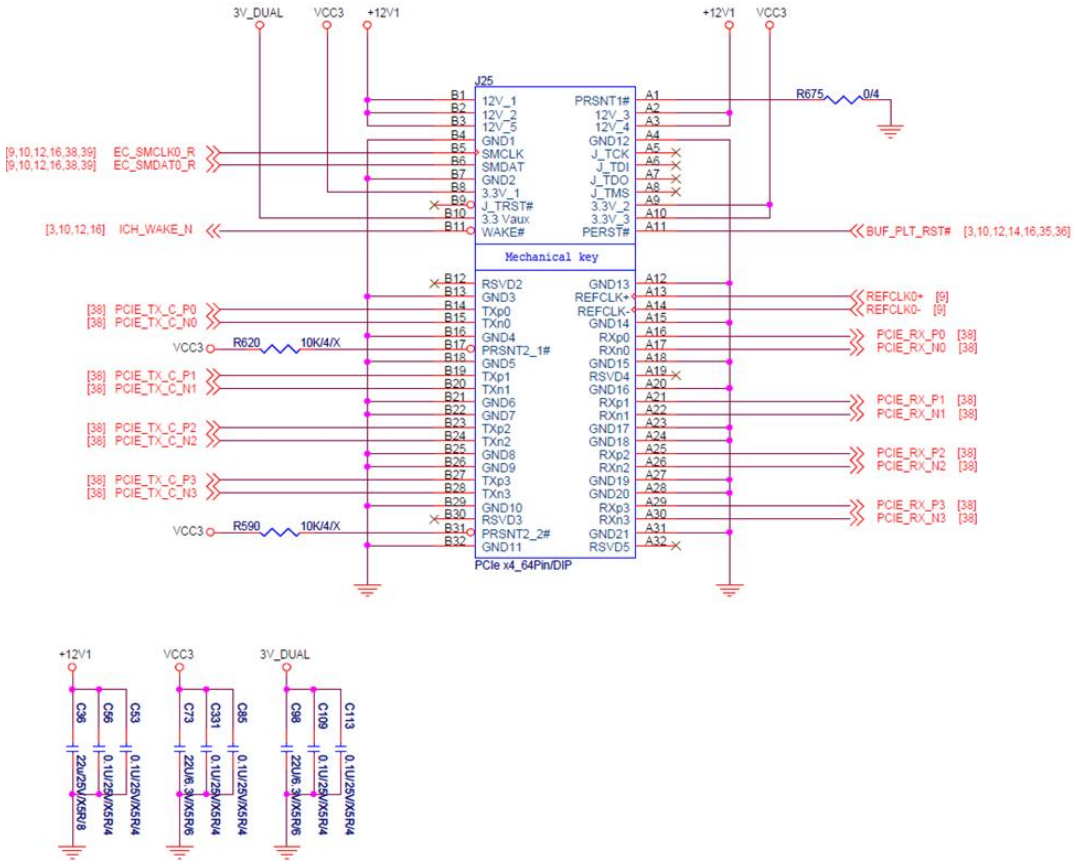


Figure 5 PCIEx4 reference schematic-2

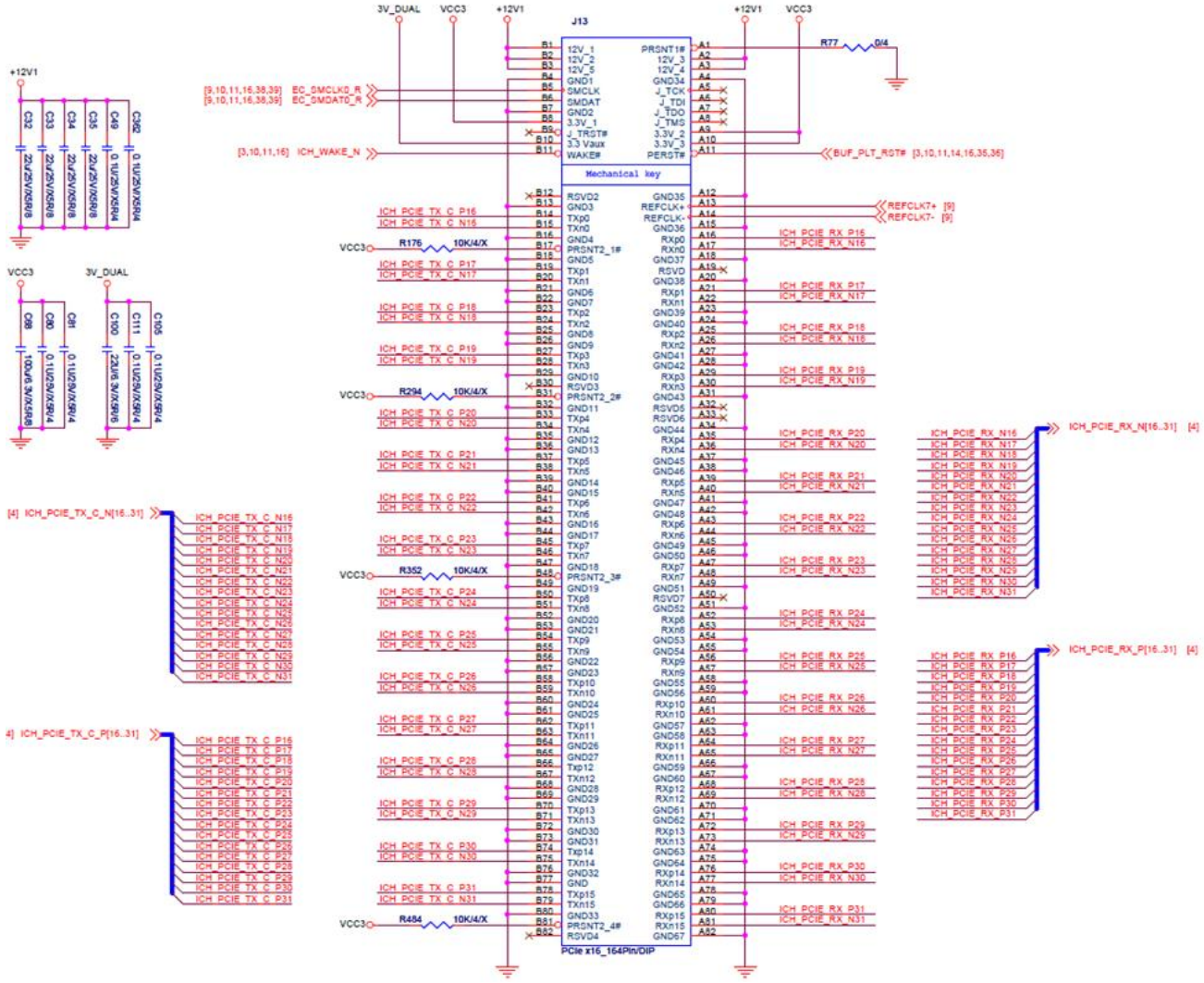


Figure 6 PCIEx16 reference schematic-3

3.1.5 Max trace length and available carrier trace length - PCIe (Device Down)

Gen 2: PIN 0~7

Gen 3: PIN 8~11, 16~31

PCIe Device Down Topology

PIN	Name	Module Length	Max Length	Available Carrier length (Device Down Topology)
A68	PCIE_TX0+	2458.03	10000	7541.97
A69	PCIE_TX0-	2457.63	10000	7542.37
A64	PCIE_TX1+	2282.57	10000	7717.43
A65	PCIE_TX1-	2283.33	10000	7716.67
A61	PCIE_TX2+	2208.4	10000	7791.6
A62	PCIE_TX2-	2209.19	10000	7790.81
A58	PCIE_TX3+	2001.87	10000	7998.13
A59	PCIE_TX3-	2001.29	10000	7998.71
A55	PCIE_TX4+	2608.64	10000	7391.36
A56	PCIE_TX4-	2609.25	10000	7390.75
A52	PCIE_TX5+	2634.39	10000	7365.61
A53	PCIE_TX5-	2634.07	10000	7365.93
D19	PCIE_TX6+	1091.22	10000	8908.78
D20	PCIE_TX6-	1091.12	10000	8908.88
D22	PCIE_TX7+	1243.99	10000	8756.01
D23	PCIE_TX7-	1245.76	10000	8754.24
A71	PCIE_TX8+	3367.03	9000	5632.97
A72	PCIE_TX8-	3366.29	9000	5633.71
A74	PCIE_TX9+	3198.56	9000	5801.44
A75	PCIE_TX9-	3199.28	9000	5800.72
A77	PCIE_TX10+	3684.24	9000	5315.76
A78	PCIE_TX10-	3683.77	9000	5316.23
A81	PCIE_TX11+	3916.79	9000	5083.21
A82	PCIE_TX11-	3917.26	9000	5082.74
A39	PCIE_TX12+	3372.62	9000	5627.38
A40	PCIE_TX12-	3372.2	9000	5627.8
A36	PCIE_TX13+	2848.31	9000	6151.69
A37	PCIE_TX13-	2848.2	9000	6151.8
A25	PCIE_TX14+	3147.16	9000	5852.84
A26	PCIE_TX14-	3147.85	9000	5852.15

A22	PCIE_TX15+	2871.22	9000	6128.78
A23	PCIE_TX15-	2872.34	9000	6127.66
D52	PCIE_TX16+	1561.51	9000	7438.49
D53	PCIE_TX16-	1562.24	9000	7437.76
D55	PCIE_TX17+	1600.46	9000	7399.54
D56	PCIE_TX17-	1600.71	9000	7399.29
D58	PCIE_TX18+	1954.47	9000	7045.53
D59	PCIE_TX18-	1954.7	9000	7045.3
D61	PCIE_TX19+	1955.88	9000	7044.12
D62	PCIE_TX19-	1955.74	9000	7044.26
D65	PCIE_TX20+	1965.51	9000	7034.49
D66	PCIE_TX20-	1965.24	9000	7034.76
D68	PCIE_TX21+	2240.59	9000	6759.41
D69	PCIE_TX21-	2240.72	9000	6759.28
D71	PCIE_TX22+	2741.58	9000	6258.42
D72	PCIE_TX22-	2741.83	9000	6258.17
D74	PCIE_TX23+	2705.88	9000	6294.12
D75	PCIE_TX23-	2705.8	9000	6294.2
D78	PCIE_TX24+	3527.5	9000	5472.5
D79	PCIE_TX24-	3526.79	9000	5473.21
D81	PCIE_TX25+	3607.5	9000	5392.5
D82	PCIE_TX25-	3608.29	9000	5391.71
D85	PCIE_TX26+	4044.31	9000	4955.69
D86	PCIE_TX26-	4044.74	9000	4955.26
D88	PCIE_TX27+	4113.17	9000	4886.83
D89	PCIE_TX27-	4113.48	9000	4886.52
D91	PCIE_TX28+	4375.95	9000	4624.05
D92	PCIE_TX28-	4375.21	9000	4624.79
D94	PCIE_TX29+	4988.59	9000	4011.41
D95	PCIE_TX29-	4988.73	9000	4011.27
D98	PCIE_TX30+	5380.61	9000	3619.39
D99	PCIE_TX30-	5380.14	9000	3619.86
D101	PCIE_TX31+	5646.21	9000	3353.79
D102	PCIE_TX31-	5645.57	9000	3354.43
B68	PCIE_RX0+	2817.46	10000	7182.54
B69	PCIE_RX0-	2817.16	10000	7182.84
B64	PCIE_RX1+	2539.32	10000	7460.68
B65	PCIE_RX1-	2539.76	10000	7460.24

B61	PCIE_RX2+	2335.1	10000	7664.9
B62	PCIE_RX2-	2334.26	10000	7665.74
B58	PCIE_RX3+	2110.09	10000	7889.91
B59	PCIE_RX3-	2110.26	10000	7889.74
B55	PCIE_RX4+	1875.44	10000	8124.56
B56	PCIE_RX4-	1875.45	10000	8124.55
B52	PCIE_RX5+	1538.25	10000	8461.75
B53	PCIE_RX5-	1538.29	10000	8461.71
C19	PCIE_RX6+	1222.5	10000	8777.5
C20	PCIE_RX6-	1222.75	10000	8777.25
C22	PCIE_RX7+	837.43	10000	9162.57
C23	PCIE_RX7-	838.56	10000	9161.44
B71	PCIE_RX8+	1902.48	9000	7097.52
B72	PCIE_RX8-	1902.2	9000	7097.8
B74	PCIE_RX9+	1747	9000	7253
B75	PCIE_RX9-	1747.29	9000	7252.71
B77	PCIE_RX10+	1856.22	9000	7143.78
B78	PCIE_RX10-	1855.71	9000	7144.29
B81	PCIE_RX11+	1840.14	9000	7159.86
B82	PCIE_RX11-	1839.28	9000	7160.72
B39	PCIE_RX12+	2316.93	9000	6683.07
B40	PCIE_RX12-	2317.62	9000	6682.38
B36	PCIE_RX13+	2166.13	9000	6833.87
B37	PCIE_RX13-	2166.3	9000	6833.7
B25	PCIE_RX14+	2412.7	9000	6587.3
B26	PCIE_RX14-	2412.77	9000	6587.23
B22	PCIE_RX15+	2149.4	9000	6850.6
B23	PCIE_RX15-	2148.91	9000	6851.09
C52	PCIE_RX16+	1275.91	9000	7724.09
C53	PCIE_RX16-	1275.86	9000	7724.14
C55	PCIE_RX17+	1495.24	9000	7504.76
C56	PCIE_RX17-	1494.81	9000	7505.19
C58	PCIE_RX18+	1657.78	9000	7342.22
C59	PCIE_RX18-	1657.77	9000	7342.23
C61	PCIE_RX19+	1854.61	9000	7145.39
C62	PCIE_RX19-	1854.53	9000	7145.47
C65	PCIE_RX20+	2142.38	9000	6857.62
C66	PCIE_RX20-	2142.5	9000	6857.5

C68	PCIE_RX21+	2671.62	9000	6328.38
C69	PCIE_RX21-	2670.83	9000	6329.17
C71	PCIE_RX22+	2966.75	9000	6033.25
C72	PCIE_RX22-	2966.63	9000	6033.37
C74	PCIE_RX23+	3084.15	9000	5915.85
C75	PCIE_RX23-	3083.68	9000	5916.32
C78	PCIE_RX24+	3248.48	9000	5751.52
C79	PCIE_RX24-	3247.77	9000	5752.23
C81	PCIE_RX25+	3431.09	9000	5568.91
C82	PCIE_RX25-	3431.63	9000	5568.37
C85	PCIE_RX26+	3737.33	9000	5262.67
C86	PCIE_RX26-	3736.8	9000	5263.2
C88	PCIE_RX27+	3986.34	9000	5013.66
C89	PCIE_RX27-	3986.99	9000	5013.01
C91	PCIE_RX28+	4306.6	9000	4693.4
C92	PCIE_RX28-	4307.19	9000	4692.81
C94	PCIE_RX29+	4582.55	9000	4417.45
C95	PCIE_RX29-	4582.16	9000	4417.84
C98	PCIE_RX30+	4959.8	9000	4040.2
C99	PCIE_RX30-	4959.7	9000	4040.3
C101	PCIE_RX31+	5212.39	9000	3787.61
C102	PCIE_RX31-	5213.11	9000	3786.89
A88	PCIE_CLK_REF+	2722.29	-	-
A89	PCIE_CLK_REF-	2721.71	-	-

Table 6 PCIE carrier available traces - Device Down

3.1.6 Max trace length and available carrier trace length - PCIe (Add In Card)

PCIe Add In Card topology

PIN	Name	Module Length	Max Length	Available Carrier length (AIC Topology)
A68	PCIE_TX0+	2458.03	10000	7541.97
A69	PCIE_TX0-	2457.63	10000	7542.37
A64	PCIE_TX1+	2282.57	10000	7717.43
A65	PCIE_TX1-	2283.33	10000	7716.67
A61	PCIE_TX2+	2208.4	10000	7791.6
A62	PCIE_TX2-	2209.19	10000	7790.81
A58	PCIE_TX3+	2001.87	10000	7998.13
A59	PCIE_TX3-	2001.29	10000	7998.71
A55	PCIE_TX4+	2608.64	10000	7391.36
A56	PCIE_TX4-	2609.25	10000	7390.75
A52	PCIE_TX5+	2634.39	10000	7365.61
A53	PCIE_TX5-	2634.07	10000	7365.93
D19	PCIE_TX6+	1091.22	10000	8908.78
D20	PCIE_TX6-	1091.12	10000	8908.88
D22	PCIE_TX7+	1243.99	10000	8756.01
D23	PCIE_TX7-	1245.76	10000	8754.24
A71	PCIE_TX8+	3367.03	7000	3632.97
A72	PCIE_TX8-	3366.29	7000	3633.71
A74	PCIE_TX9+	3198.56	7000	3801.44
A75	PCIE_TX9-	3199.28	7000	3800.72
A77	PCIE_TX10+	3684.24	7000	3315.76
A78	PCIE_TX10-	3683.77	7000	3316.23
A81	PCIE_TX11+	3916.79	7000	3083.21
A82	PCIE_TX11-	3917.26	7000	3082.74
A39	PCIE_TX12+	3372.62	7000	3627.38
A40	PCIE_TX12-	3372.2	7000	3627.8
A36	PCIE_TX13+	2848.31	7000	4151.69
A37	PCIE_TX13-	2848.2	7000	4151.8
A25	PCIE_TX14+	3147.16	7000	3852.84
A26	PCIE_TX14-	3147.85	7000	3852.15
A22	PCIE_TX15+	2871.22	7000	4128.78
A23	PCIE_TX15-	2872.34	7000	4127.66

D52	PCIE_TX16+	1561.51	7000	5438.49
D53	PCIE_TX16-	1562.24	7000	5437.76
D55	PCIE_TX17+	1600.46	7000	5399.54
D56	PCIE_TX17-	1600.71	7000	5399.29
D58	PCIE_TX18+	1954.47	7000	5045.53
D59	PCIE_TX18-	1954.7	7000	5045.3
D61	PCIE_TX19+	1955.88	7000	5044.12
D62	PCIE_TX19-	1955.74	7000	5044.26
D65	PCIE_TX20+	1965.51	7000	5034.49
D66	PCIE_TX20-	1965.24	7000	5034.76
D68	PCIE_TX21+	2240.59	7000	4759.41
D69	PCIE_TX21-	2240.72	7000	4759.28
D71	PCIE_TX22+	2741.58	7000	4258.42
D72	PCIE_TX22-	2741.83	7000	4258.17
D74	PCIE_TX23+	2705.88	7000	4294.12
D75	PCIE_TX23-	2705.8	7000	4294.2
D78	PCIE_TX24+	3527.5	7000	3472.5
D79	PCIE_TX24-	3526.79	7000	3473.21
D81	PCIE_TX25+	3607.5	7000	3392.5
D82	PCIE_TX25-	3608.29	7000	3391.71
D85	PCIE_TX26+	4044.31	7000	2955.69
D86	PCIE_TX26-	4044.74	7000	2955.26
D88	PCIE_TX27+	4113.17	7000	2886.83
D89	PCIE_TX27-	4113.48	7000	2886.52
D91	PCIE_TX28+	4375.95	7000	2624.05
D92	PCIE_TX28-	4375.21	7000	2624.79
D94	PCIE_TX29+	4988.59	7000	2011.41
D95	PCIE_TX29-	4988.73	7000	2011.27
D98	PCIE_TX30+	5380.61	7000	1619.39
D99	PCIE_TX30-	5380.14	7000	1619.86
D101	PCIE_TX31+	5646.21	7000	1353.79
D102	PCIE_TX31-	5645.57	7000	1354.43
A88	PCIE_CLK_REF+	2722.29	-	-
A89	PCIE_CLK_REF-	2721.71	-	-

Table 7 PCIE carrier available traces - Add In Card

3.2 USB 2.0/3.0

PCOM- B700G-NS USB2.0

Pin#	Pin Name	COMe 3.0 Specification (Signals Requiring Module Termination)	Pin Typ	B700G-NS Module	Pwr Rail /Tolerance(Volt)
A45	USB0-	No termination is required on USB pairs.	I/O USB	SoC to Com Express Row connector.	3.3V Suspend/3.3V
A46	USB0+				
B45	USB1-				
B46	USB1+				
A42	USB2-				
A43	USB2+				
B42	USB3-				
B43	USB3+				
B44	USB_0_1_OC#	Pulled up to 3.3V standby on module with a 10K Ω resistor	I CMOS	PU 10k ohm to +3V_Dual	3.3V Suspend/3.3V
A44	USB_2_3_OC#				

Table 8 B700G-NS USB 2.0

PCOM- B700G-NS USB3.0

Pin#	Pin Name	COMe 3.0 Specification (Signals Requiring Module Termination)	Pin Typ	B700G-NS Module	Pwr Rail /Tolerance(Volt)
C3	USB_SSRX0-	AC coupled off Module.	I PCIE	SoC to Com Express Row connector.	AC coupled off Module.
C4	USB_SSRX0+				
C6	USB_SSRX1-				
C7	USB_SSRX1+				
C9	USB_SSRX2-				
C10	USB_SSRX2+				
C12	USB_SSRX3-				
C13	USB_SSRX3+				
D3	USB_SSTX0-	AC coupled on Module.	O PCIE	0.1uF AC coupled on the Module(Gen3).	AC coupled on Module
D4	USB_SSTX0+				
D6	USB_SSTX1-				
D7	USB_SSTX1+				
D9	USB_SSTX2-				
D10	USB_SSTX2+				
D12	USB_SSTX3-				
D13	USB_SSTX3+				

Table 9 B700G-NS USB 3.0

3.2.1 PCB layout guideline - USB2.0/3.0

Parameter	Trace Routing	Trace Routing
Transfer rate / Port	480 Mbit/s	5.0 Gbit/s
Maximum signal line length (coupled traces)	Max. 12.0 inches	Max. 8 inches/
Differential Impedance	85 Ω +/-12%	85 Ω +/-12%
Single-ended Impedance	50 Ω +/-12%	50 Ω +/-12%
Trace width (W)	3.5 mil PCB stack-up dependent	3.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4 mil PCB stack-up dependent	4mil PCB stack-up dependent
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 15mils	Min. 15mils
Spacing between differential pairs	Min. 15mils	Min. 15mils
Length matching between differential pairs (intra-pair)	5 mils	5 mils
Reference plane	GND referenced preferred	GND referenced preferred
Spacing from edge of plane	Min. 10*W mils (W=trace width)	Min. 10*W mils (W=trace width)
Via Usage	Max. 1 vias	Max. 1 vias

Table 10 USB 2.0 / 3.0 Layout information

3.2.2 Reference schematic - PCOM-C701 ZR1

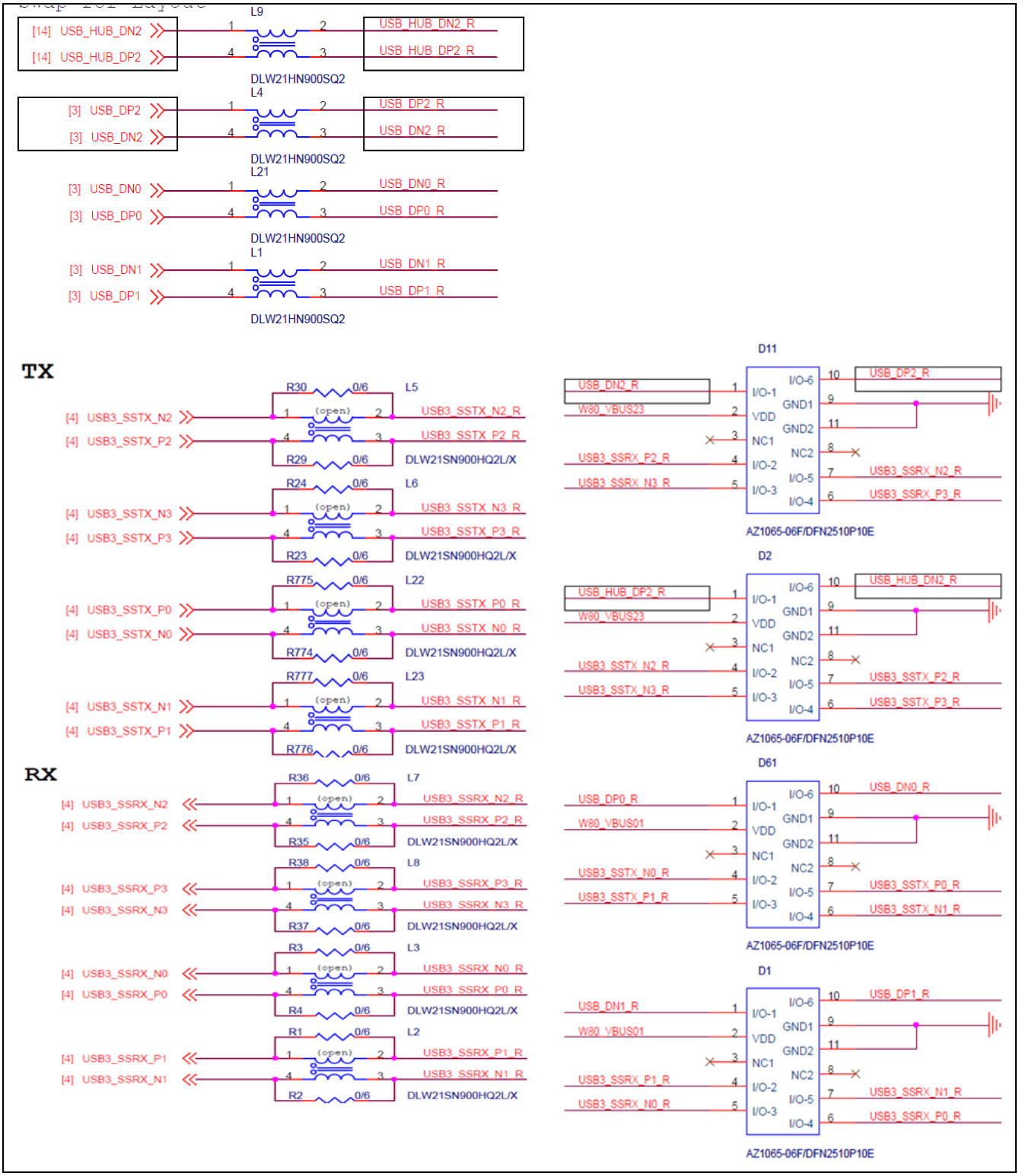


Figure 7 USB 2.0 / 3.0 Reference schematic 1

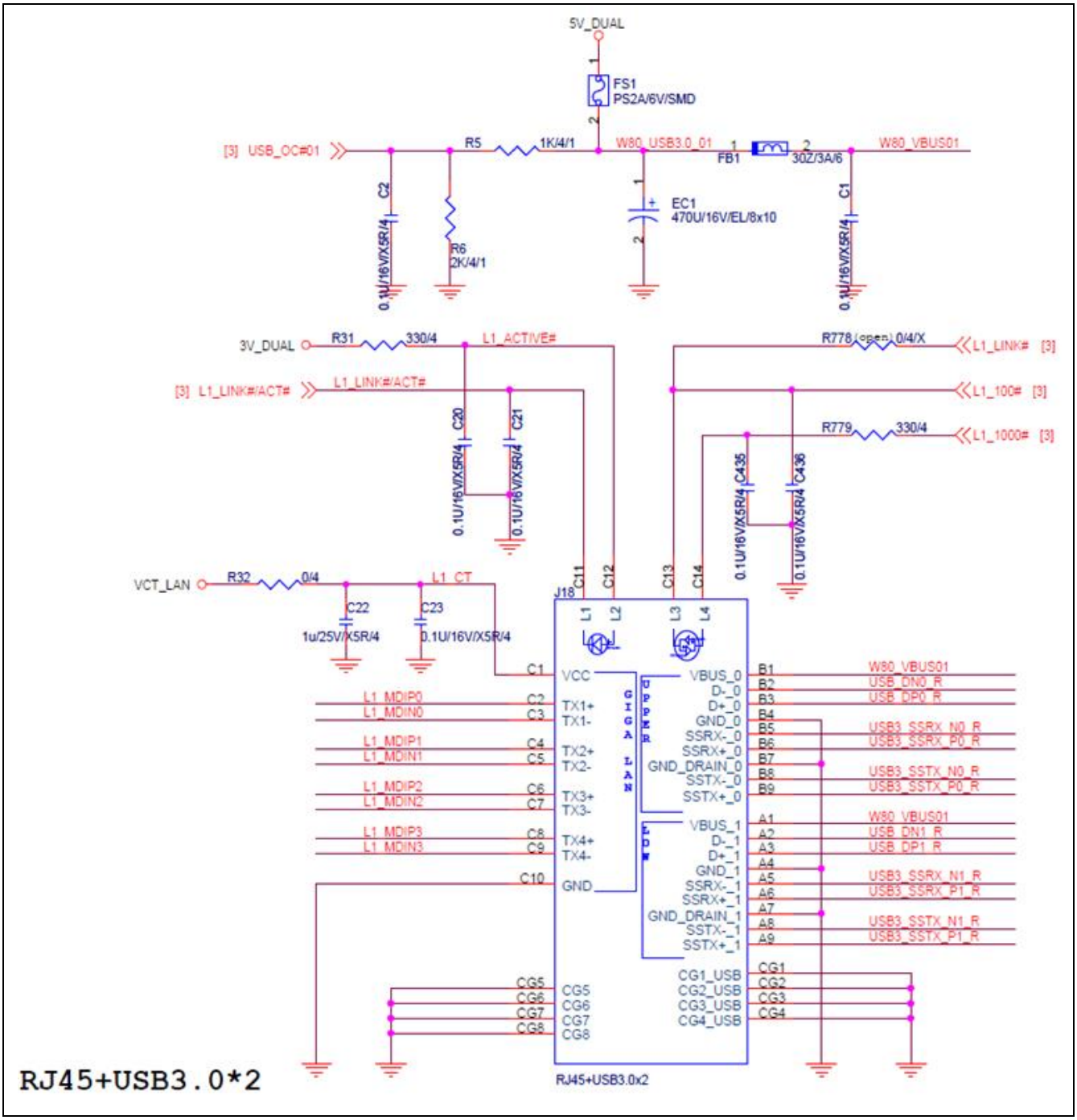


Figure 8 USB 2.0 / 3.0 Reference schematic 2

3.2.3 Max trace length and available carrier trace length - USB 2.0 / 3.0

PIN	Name	Module Length	Max Length	Available Carrier length
A45	USB0-	1413.63	12000	10586.37
A46	USB0+	1414.59	12000	10585.41
B45	USB1-	1897.66	12000	10102.34
B46	USB1+	1898.2	12000	10101.8
A42	USB2-	1383	12000	10617
A43	USB2+	1382.58	12000	10617.42
B42	USB3-	1477.54	12000	10522.46
B43	USB3+	1478.07	12000	10521.93
C3	USB_SSRX0-	1941.17	8000	6058.83
C4	USB_SSRX0+	1940.63	8000	6059.37
C6	USB_SSRX1-	1755.1	8000	6244.9
C7	USB_SSRX1+	1754.78	8000	6245.22
C9	USB_SSRX2-	1697.54	8000	6302.46
C10	USB_SSRX2+	1697.17	8000	6302.83
C12	USB_SSRX3-	1627.85	8000	6372.15
C13	USB_SSRX3+	1627.45	8000	6372.55
D3	USB_SSTX0-	1538.6	8000	6461.4
D4	USB_SSTX0+	1538.29	8000	6461.71

Table 11 Carrier available traces - USB 2.0 / 3.0

3.3 GbE LAN

PCOM-B700G-NS LAN

Pin#	Pin Name	COM e 2.0/2.1 Specification (Signals Requiring Module Termination)	Pin Typ	B700G-NS Module	Pwr Rail /Tolerance(Volt)
A12	GBE0_MDI0-	-	I/O Analog	Media Dependent Interface signal. I210 chip on Module.	3.3V max Suspend
A13	GBE0_MDI0+				
A9	GBE0_MDI1-				
A10	GBE0_MDI1+				
A6	GBE0_MDI2-				
A7	GBE0_MDI2+				
A2	GBE0_MDI3-				
A3	GBE0_MDI3+				
A8	GBE0_LINK#	-	OD CMOS	Gigabit Ethernet Controller 0 link indicator, active low.	3.3V Suspend/3.3V
A4	GBE0_LINK100#	-	OD CMOS	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	3.3V Suspend/3.3V
A5	GBE0_LINK1000#	-	OD CMOS	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	3.3V Suspend/3.3V
A14	GBE0_CTREF	-	REF	Reserved resistor NP (Reference voltage for Carrier Board Ethernet channel 0 magnetics center	GND min 3.3V max
B2	GBE0_ACT#	-	OD CMOS	I210 chip to Com Express Row connector.	3.3V Suspend/3.3V

Table 12 B700G-NS LAN

3.3.1 PCB layout guideline - LAN

Parameter	Trace Routing
Differential Impedance	100 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%
Trace width (W)	4 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	9 mil PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 28 mils
Length matching between RX and TX pairs (inter-pair)	Max. 10mils
Spacing from edge of plane	Min. 10*W mils (W=trace width)

Table 13 LAN Layout information

3.3.2 Reference schematic - PCOM-C701 ZR1

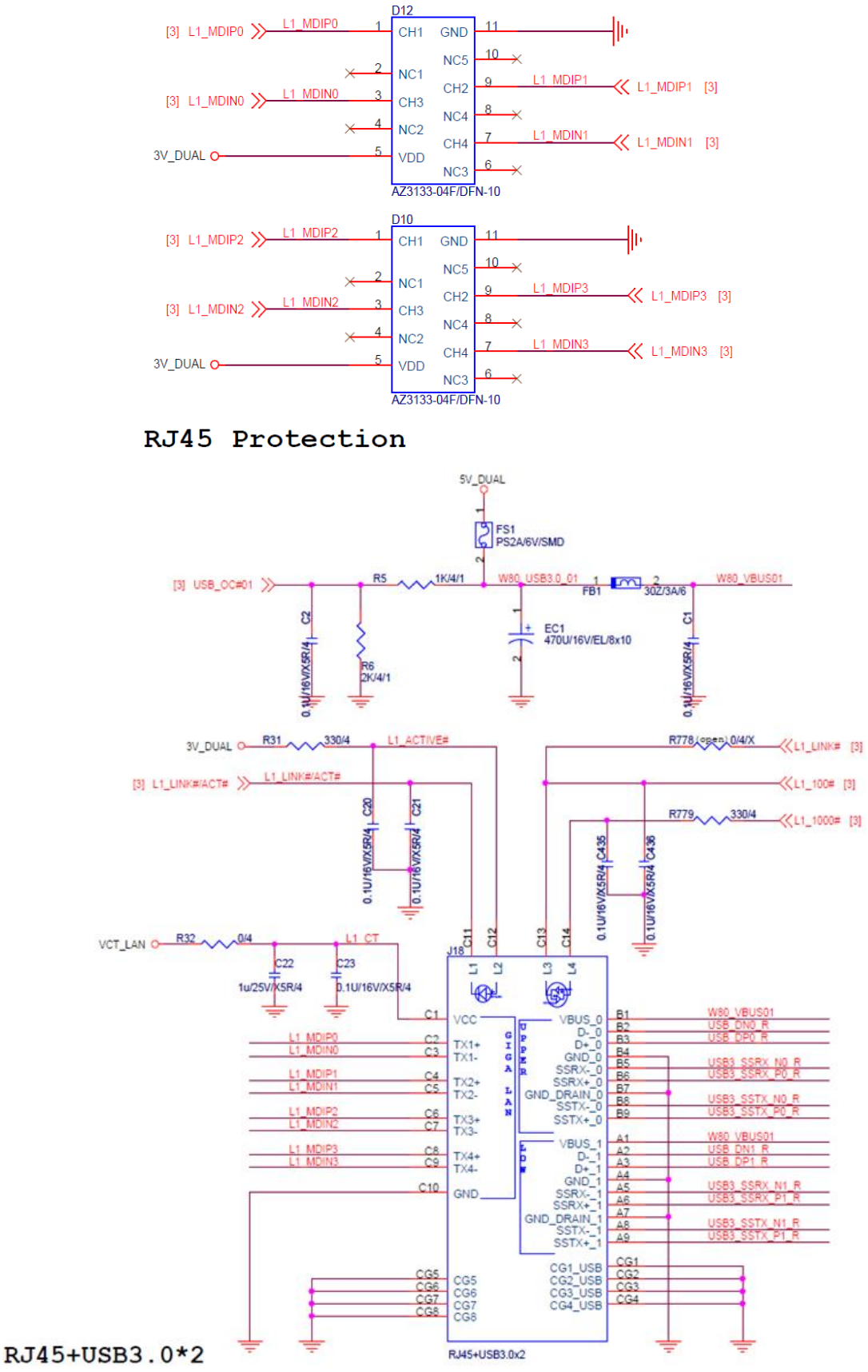


Figure 9 Reference schematic – LAN

3.3.3 Max trace length and available carrier trace length -

LAN

PIN	Name	Module Length	Max Length	Available Carrier length
A13	GBE0_MDI0+	1582.03	5000	3417.97
A12	GBE0_MDI0-	1581.46	5000	3418.54
A10	GBE0_MDI1+	1582.15	5000	3417.85
A9	GBE0_MDI1-	1581.67	5000	3418.33
A7	GBE0_MDI2+	1583.39	5000	3416.61
A6	GBE0_MDI2-	1583.01	5000	3416.99
A3	GBE0_MDI3+	1582.69	5000	3417.31
A2	GBE0_MDI3-	1583.27	5000	3416.73

Table 14 Carrier available traces - LAN

3.4 SATA

PCOM-B700G-NS SATA

Pin#	Pin Name	COMe 3.0 Specification (Signals Requiring Module Termination)	Pin Typ	B700G-NS Module	Pwr Rail /Tolerance(Volt)
A16	SATA0_TX+	AC coupled on the Module	O SATA	0.01uF AC coupled on the Module(Gen3).	AC coupled on Module
A17	SATA0_TX-				
A19	SATA0_RX+		I SATA		
A20	SATA0_RX-				
B16	SATA1_TX+		O SATA		
B17	SATA1_TX-				
B19	SATA1_RX+		I SATA		
B20	SATA1_RX-				
A28	(S)ATA_ACT#		O/D(I/O) CMOS	PU 4.7k ohm to +P3V3S	3.3V / 3.3V
B18	SUS_STAT#	Indicates imminent suspend operation; used to notify LPC devices	O CMOS	-	3.3VSuspend/ 3.3V

Table 15 B700G-NS SATA

3.4.1 PCB layout guideline -SATA

Parameter	Trace Routing
Transfer Rate	Up to 6.0 Gbit/s
Maximum signal line length (coupled traces)	5.0 inches
Differential Impedance	85 Ω +/-12%
Single-ended Impedance	50 Ω +/-12%
Trace width (W)	4 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4.5mil PCB stack-up dependent
Spacing between differential pairs and high-speed periodic signals	Min. 20 mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Spacing from edge of plane	Min. 10*W mils (W=trace width)
Via Usage	A maximum of 1 vias is recommended.
AC Coupling capacitors	10nF

Table 16 SATA layout information

3.4.2 Reference schematic - PCOM-C701 ZR1

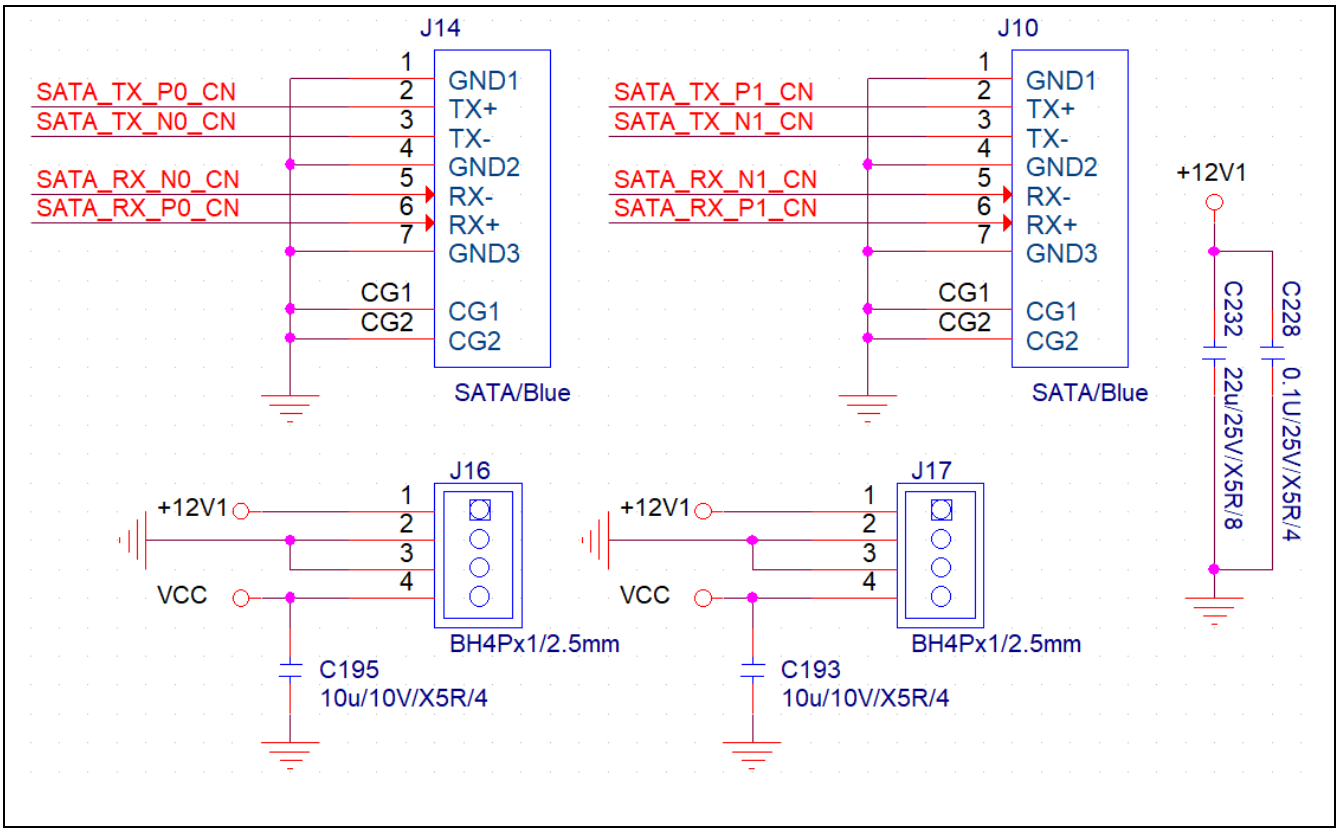


Figure 10 Reference schematic –SATA

3.4.3 Max trace length and available carrier trace length - SATA

PIN	Name	Module Length	Max Length	Available Carrier length
A16	SATA0_TX+	3994.75	5000	1005.25
A17	SATA0_TX-	3995.51	5000	1004.49
A19	SATA0_RX+	4027.88	5000	972.12
A20	SATA0_RX-	4028.27	5000	971.73
B16	SATA1_TX+	3576.69	5000	1423.31
B17	SATA1_TX-	3576.24	5000	1423.76
B19	SATA1_RX+	3486.85	5000	1513.15
B20	SATA1_RX-	3486.4	5000	1513.6

Table 17 Carrier available traces - SATA

3.5 NCSI

PCOM-B700G-NS NCSI

Pin#	Pin Name	Description	Pin Typ	B700G-NS Module follow intel	Pwr Rail /Tolerance(Volt)
A84	NCSI_TX_EN	NC-SI Transmit enable.	I CMOS	PD 10k ohm to GND	3.3V Suspend /3.3V
B91	NCSI_CLK_IN	NC-SI Clock reference for receive, transmit, and control interface			
B95	NCSI_TXD1	NC-SI Transmit Data		PU 10k ohm V_3P3M	
B96	NCSI_TXD0				
B98	NCSI_ARB_IN	NC-SI hardware arbitration input.		–	
B99	NCSI_ARB_OUT	NC-SI hardware arbitration output.	O CMOS		
B92	NCSI_RXD1	NC-SI Receive Data		PU 10k ohm V_3P3M	
B93	NCSI_RXD0				
B94	NCSI_CRS_DV	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.		PD 10k ohm to GND	

Table 18 B700G-NS NCSI

3.5.1 PCB layout guideline - NCSI

Parameter	Trace Routing
when using 4-point multi drop connections	6.5 inches
when using a point-to-point connection to the MC.	8 inches
Single-ended Impedance	50 Ω+/-10%
Trace width (W)	PCB stack-up dependent
Trace-to-trace space	12 mils (3h) PCB stack-up dependent

Table 19 NCSI Layout information

Note:

1. The clock-to-data signals length match should be done using the NC-SI timing analysis spreadsheet to ensure the timing restrictions are met while maintaining the routing length for both clock and data paths below the maximum values specified.
2. Intel I210 Layout check list NCSI recommend : total skew from the clock source to all devices should be less than 1 ns (less than or equal to ~5.5 inches trace length skew).

3.5.2 Max trace length and available carrier trace length - NCSI

PIN	Name	Module Length	Max Length	Available Carrier length
A84	NCSI_TX_EN	4641.34	8000	3358.66
B95	NCSI_TXD1	4864.81	8000	3135.19
B96	NCSI_TXD0	4867.42	8000	3132.58
B92	NCSI_RXD1	5091.34	8000	2908.66
B93	NCSI_RXD0	4637.02	8000	3362.98
B94	NCSI_CRS_DV	4815.23	8000	3184.77
B91	NCSI_CLK_IN	4764.42	12000	7235.58

Table 20 Carrier available traces – NCSI

3.6 10GbE LAN

Pin#	Pin Name	Description	Pin Typ	B700G-NS Module	Pwr Rail /Tolerance(Volt)
D49	10G_KR_TX0+	10GBASE-KR ports, transmit output differential pairs.	O KR	–	AC coupled at receiver
D50	10G_KR_TX0-				
D42	10G_KR_TX1+				
D43	10G_KR_TX1-				
D29	10G_KR_TX2+				
D30	10G_KR_TX2-				
D26	10G_KR_TX3+				
D27	10G_KR_TX3-				
C49	10G_KR_RX0+	10GBASE-KR ports, receive input differential pairs.	I KR	0.1uF AC coupled on the Module	AC coupled on Module
C50	10G_KR_RX0-				
C42	10G_KR_RX1+				
C43	10G_KR_RX1-				
C29	10G_KR_RX2+				
C30	10G_KR_RX2-				
C26	10G_KR_RX3+				
C27	10G_KR_RX3-				
D39	10G_SFP_SCL0	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O OD CMOS	reserve PU 2.2k ohm to +3V_Dual	3.3V Suspend /3.3V
D38	10G_SFP_SCL1				
D33	10G_SFP_SCL2				
D32	10G_SFP_SCL3				
C38	10G_SFP_SDA0	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O OD CMOS	reserve PU 2.2k ohm to +3V_Dual	3.3V Suspend /3.3V
C39	10G_SFP_SDA1				
C33	10G_SFP_SDA2				
C32	10G_SFP_SDA3				
C46	10G_PHY_MDC_SCL0	**MDIO Mode:** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY.	O CMOS	reserve PU 2.2k ohm to +3V_Dual	3.3V Suspend /3.3V
C45	10G_PHY_MDC_SCL1			PU 1k ohm to +3V_Dual for LED	
C16	10G_PHY_MDC_SCL2	**I2C Mode:** I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD CMOS	reserve PU 2.2k ohm to +3V_Dual for	
C15	10G_PHY_MDC_SCL3			PU 12.1k ohm to +3V_Dual for LED	

Table 21 B700G-NS 10GbE LAN

Pin#	Pin Name	Description	Pin Typ	B700G-NS Module	Pwr Rail /Tolerance(Volt)
D46	10G_PHY_MDIO_SDA0	**MDIO Mode:** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY. --- **I2C Mode:** I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	O CMOS --- I/O OD CMOS	reserve PU 2.2k ohm to +3V_Dual	3.3V Suspend /3.3V
D45	10G_PHY_MDIO_SDA1			PU 1k ohm to +3V_Dual for LED	
D16	10G_PHY_MDIO_SDA2			reserve PU 2.2k ohm to +3V_Dual for	
D15	10G_PHY_MDIO_SDA3			PU 12.1k ohm to +3V_Dual for LED	
D35	10G_PHY_SEL_01	Phy mode select pin: If high Phy0 and Phy1 are configured by MDIO. If low Phy2 and Phy3 are configured by I2C. For MDIO mode, this pin should be left not connected on the Carrier.	I CMOS	PU 10k ohm +3V_Dual	3.3V Suspend /3.3V
D34	10G_PHY_SEL_23				
C35	10G_PHY_RST_01	Output signal that resets an optical PHY on port 0 and port1 (with copper PHY this signal is not used).	O CMOS	PU 4.7k ohm +3V_Dual	3.3V Suspend /3.3V
C34	10G_PHY_RST_23				
C40	10G_SDP0	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signa	I/O CMOS	PU 1k ohm +3V_Dual	3.3V Suspend /3.3V
D40	10G_SDP1				
C17	10G_SDP2				
D17	10G_SDP3				
C47	10G_INT0	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.	I CMOS	PU 1k ohm +3V_Dual	3.3V Suspend /3.3V
D47	10G_INT1				
C24	10G_INT2				
D24	10G_INT3				
C36	10G_LED_SDA	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs.	I/O OD CMOS	reserve PU 2.2k ohm to +3V_Dual for	3.3V Suspend /3.3V
C37	10G_LED_SCL	I2C Clock,of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs			

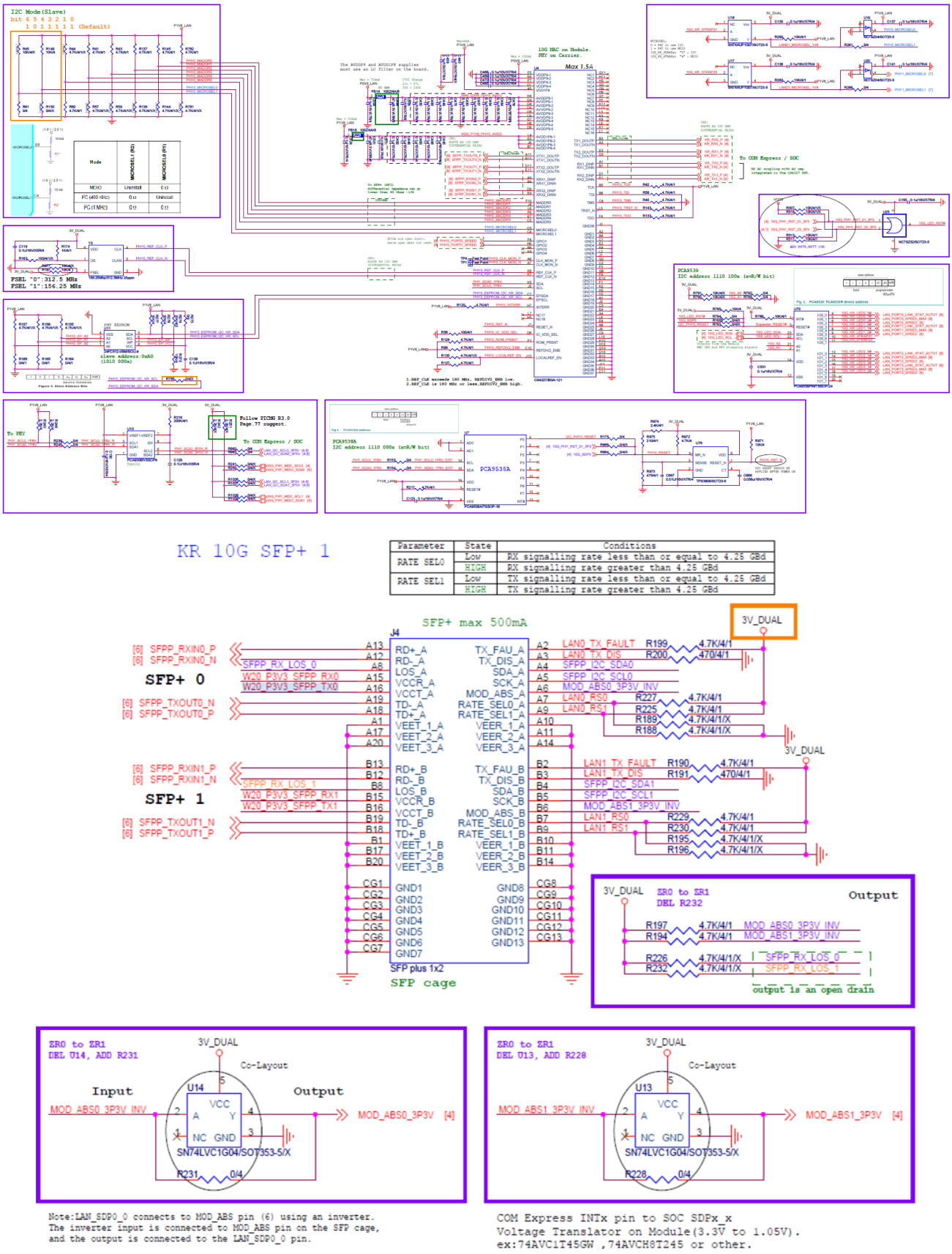
Table 22 B700G-NS 10GbE LAN

3.6.1 PCB layout guideline -10GbE LAN

Parameter	Trace Routing
Differential Impedance	100 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%
Trace width (W)	3.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	8 mil PCB stack-up dependent
Inter-pair Spacing Like Pairs (Tx to Tx or Rx to Rx)	15mail (5h) with Striplineh 36mail (12h) with Microstrip PCB stack-up dependent
Spacing to other signals (Tx to Rx)	21mail (7h) with Striplineh 45mail (15h) with Microstrip PCB stack-up dependent
Length matching between differential pairs (intra-pair)	Max. 5mils
Via stub length (max)	20 mils

Table 23 10GbE LAN layout information

3.6.2 Reference schematic - PCOM-C701 ZR1



Parameter	State	Conditions
RATE SEL0	Low	RX signalling rate less than or equal to 4.25 GBd
	HIGH	RX signalling rate greater than 4.25 GBd
RATE SEL1	Low	TX signalling rate less than or equal to 4.25 GBd
	HIGH	TX signalling rate greater than 4.25 GBd

Figure 11 Reference schematic – 10GbE LAN

3.6.3 Max trace length and available carrier trace length - 10GbE LAN

PIN	Name	Module Length	Max Length	Available Carrier length
D49	10G_KR_TX0+	2193.84	8000	5806.16
D50	10G_KR_TX0-	2193.81	8000	5806.19
D42	10G_KR_TX1+	2223.99	8000	5776.01
D43	10G_KR_TX1-	2224.35	8000	5775.65
D29	10G_KR_TX2+	2258.22	8000	5741.78
D30	10G_KR_TX2-	2257.6	8000	5742.4
D26	10G_KR_TX3+	2463.68	8000	5536.32
D27	10G_KR_TX3-	2462.94	8000	5537.06
C49	10G_KR_RX0+	2631.47	8000	5368.53
C50	10G_KR_RX0-	2632.14	8000	5367.86
C42	10G_KR_RX1+	2723.56	8000	5276.44
C43	10G_KR_RX1-	2724.3	8000	5275.7
C29	10G_KR_RX2+	2782.2	8000	5217.8
C30	10G_KR_RX2-	2782.29	8000	5217.71
C26	10G_KR_RX3+	2549.33	8000	5450.67
C27	10G_KR_RX3-	2549.57	8000	5450.43

Table 24 Carrier available traces - 10GbE LAN

3.7 UART

PCOM- B700G-NS UART

Pin#	Pin Name	Description	Pin Typ	B700G-NS Module	Pwr Rail /Tolerance(Volt)
A98	SER0_TX	General purpose serial port transmitter	O CMOS	Series connection Schottky diode	5V / 12V
A99	SER0_RX	General purpose serial port receiver	I CMOS		
A101	SER1_TX	General purpose serial port transmitter / CAN_TX	O CMOS		
A102	SER1_RX	General purpose serial port receiver / CAN_RX	I CMOS		

Table 25 B700G-NS UART

3.7.1 Reference schematic - PCOM-C701 ZR1

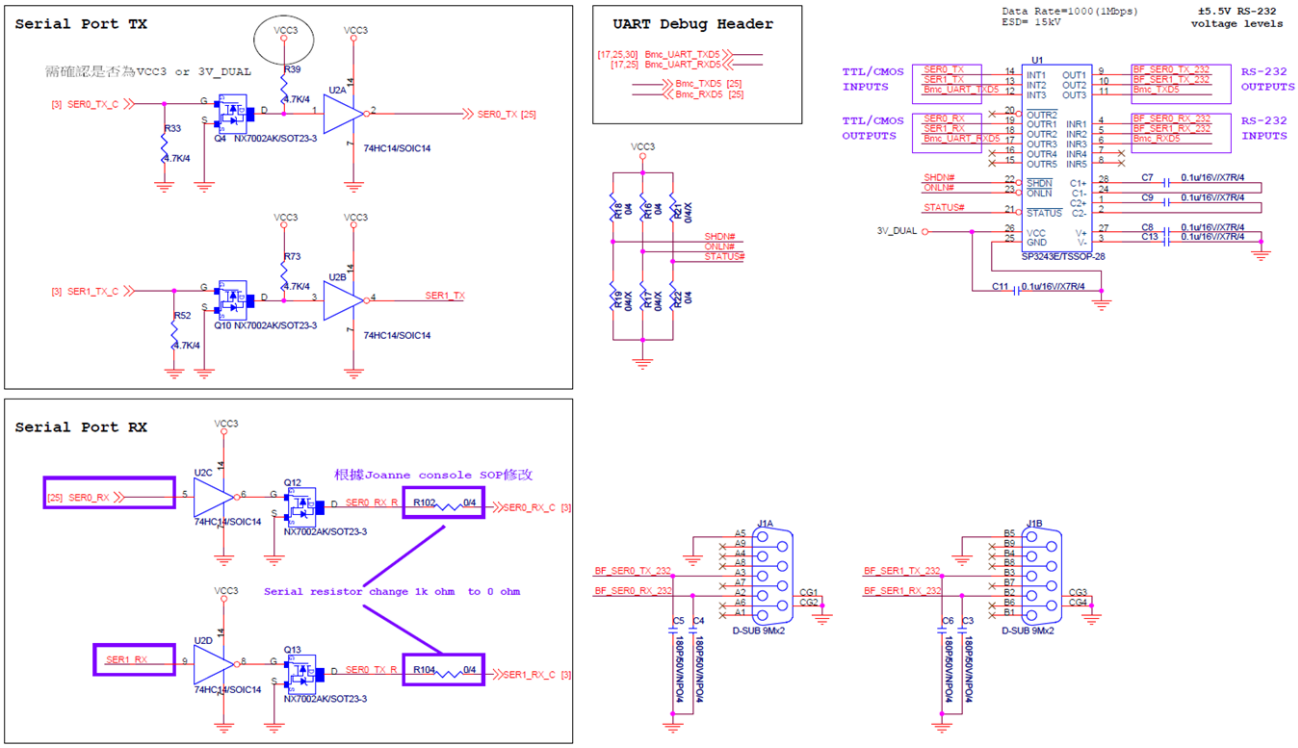


Figure 12 Reference schematic –UART

3.8 I2C

PCOM-B700G-NS I2C

Pin#	Pin Name	Description	Pin Typ	B700G-NS Module	Pwr Rail /Tolerance(Volt)
B33	I2C_CLK	General purpose I2C port clock output	I/O OD CMOS	PU 2.2k ohm to +3V_Dual.	3.3V Suspend/ 3.3V
B34	I2C_DAT	General purpose I2C port data I/O line			

Table 26 B700G-NS I2C

3.9 SMBus

PCOM- B700G-NS SMBus

Pin#	Pin Name	Description	Pin Typ	B700G-NS Module	Pwr Rail /Tolerance(Volt)
B13	SMB_CK	System Management Bus bidirectional clock line	I/O OD CMOS	PU 4.7K ohm to +3V_Dual.	3.3V Suspend/ 3.3V
B14	SMB_DAT	System Management Bus bidirectional data line			
B15	SMB_ALERT#	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I CMOS		

Table 27 B700G-NS SMBus

3.10 GPIO

PCOM- B700G-NS GPIO

Pin#	Pin Name	Description	Pin Typ	B700G-NS Module	Pwr Rail /Tolerance(Volt)
A54	GPI0	General purpose input pins. Pulled high internally on the Module.	I CMOS	PU 10k ohm to +P3V3S .	3.3V/3.3V
A63	GPI1				
A67	GPI2				
A85	GPI3				
A93	GPO0	–	O CMOS	EC to Com Express Row connector.	3.3V/ 3.3V
B54	GPO1				
B57	GPO2				
B63	GPO3				

Table 28 B700G-NS GPIO

3.11 LPC

PCOM-B700G-NS LPC

Pin#	Pin Name	Description	Pin Typ	B700G-NS Module	Pwr Rail /Tolerance(Volt)
A50	LPC_SERIRQ	LPC Mode: LPC serial interrup	I/O CMOS	PU 10k ohm to +P3V3S	3.3V/3.3V
B3	LPC_FRAME#	LPC frame indicates the start of an LPC cycle	O CMOS	Series connection 33 ohm	
B4	LPC_AD0	LPC Mode: LPC multiplexed address, command and data bus	I/O CMOS		
B5	LPC_AD1				
B6	LPC_AD2				
B7	LPC_AD3				
B8	LPC_DRQ0#	LPC Mode: LPC serial DMA request	I CMOS	-	
B9	LPC_DRQ1#				
B10	LPC_CLK	LPC clock output - 33MHz nominal	O CMOS	Series connection 22 ohm (Intel CRB)	

Table 29 B700G-NS LPC

3.11.1 Reference schematic - PCOM-C701 ZR1

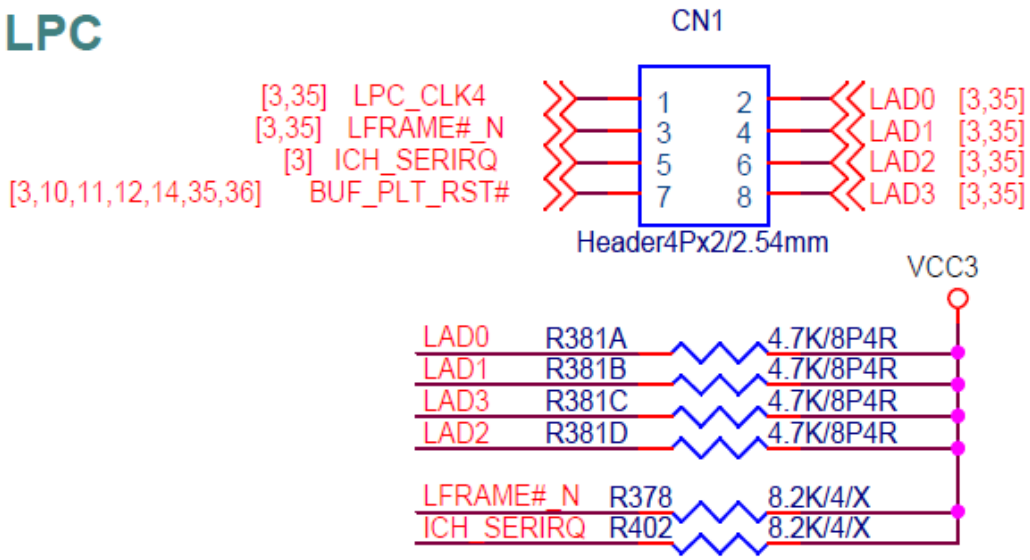


Figure 13 Reference schematic –LPC

3.12 SPI

An external SPI BIOS is designed on the Carrier board, which allows the Module boot from the Carrier SPI BIOS. To achieve this function, the BIOS_DIS0# and BIOS_DIS1# must be designed as a selectable method on the Carrier.

PCOM-B700G-NS SPI

Pin#	Pin Name	Description	Pin Typ	B700G-NS Module	Pwr Rail /Tolerance(Volt)
A34	BIOS_DIS0#	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low	I CMOS	PU 10k ohm to +3V_Dual	NA
B88	BIOS_DIS1#				
A91	SPI_POWER	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER	O	+3V_Dual	3.3V Suspend/ 3.3V
A92	SPI_MISO	Data in to Module from Carrier SPI	I CMOS	33 ohm series connection (Intel PDG)	
A95	SPI_MOSI	Data out from Module to Carrier SPI	O CMOS		
A94	SPI_CLK	Clock from Module to Carrier SPI			
B97	SPI_CS#	–	O CMOS	–	

Table 30 PCOM-B700G-NS SPI

3.12.1 Reference schematic - PCOM-C605 R0

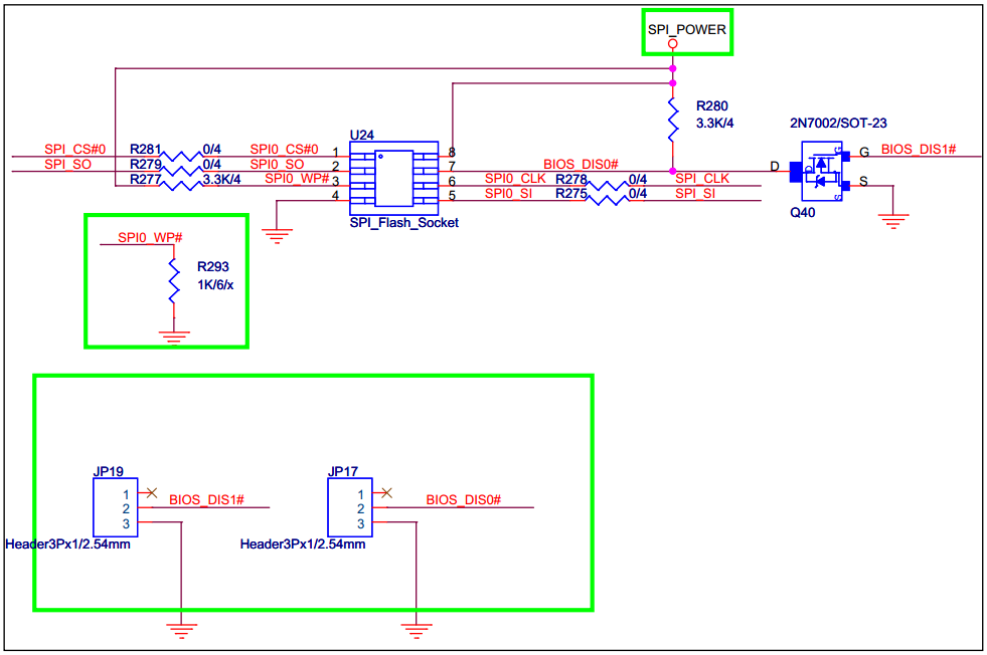


Figure 14 Reference schematic –SPI

4 Power

PCOM-B700G-NS is designed for both AT (default, AC Power loss ON) and ATX power mode, which depends on the power mode design on carrier board. The following ATX and AT mode power sequences are provided for the carrier design guideline.

4.1 Power sequence

The AT power sequence is based on PCOM-B700G-NS with evaluation carrier PCOM-C701-ZR1

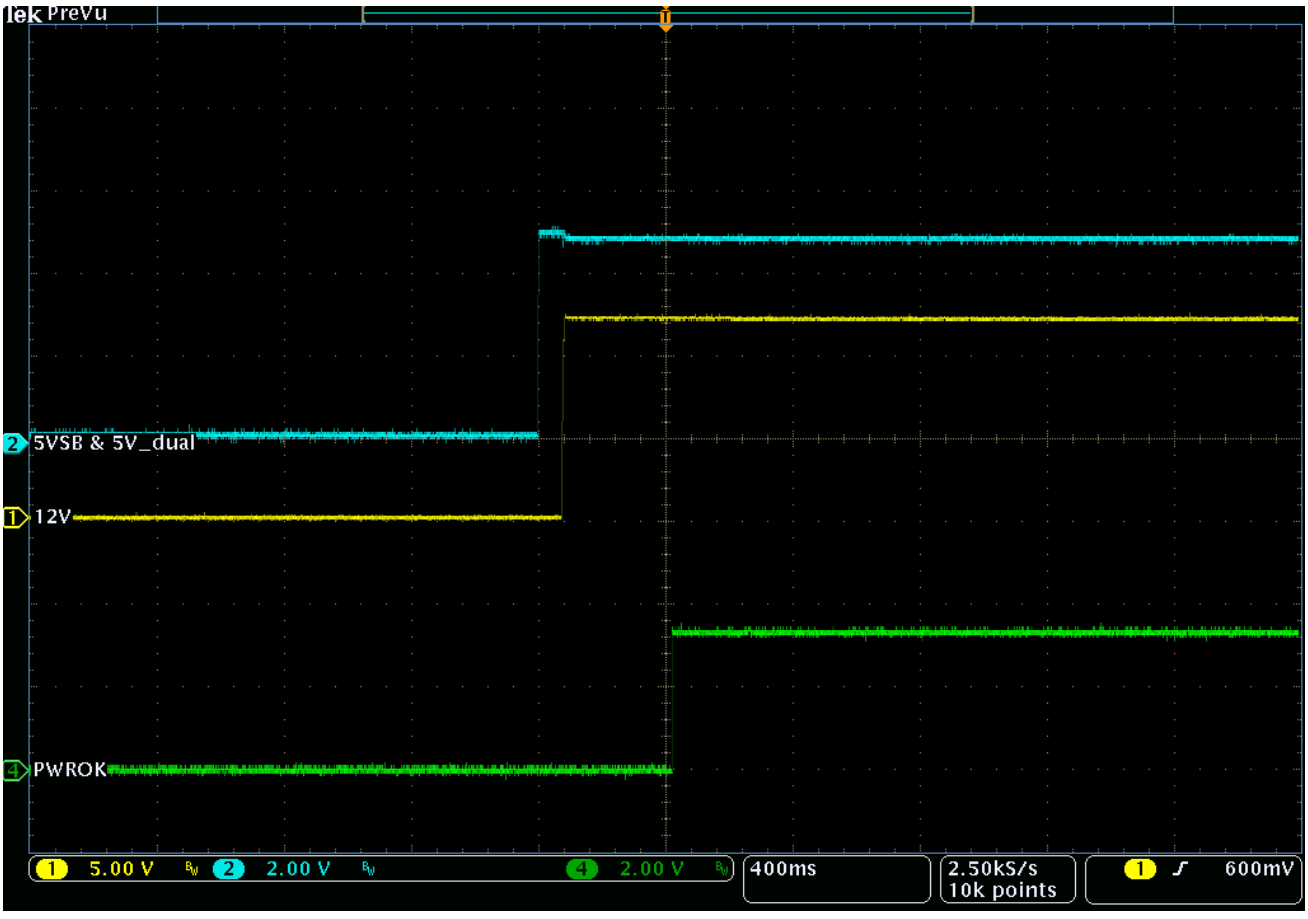


Figure 15 Power Sequence under AT Mode

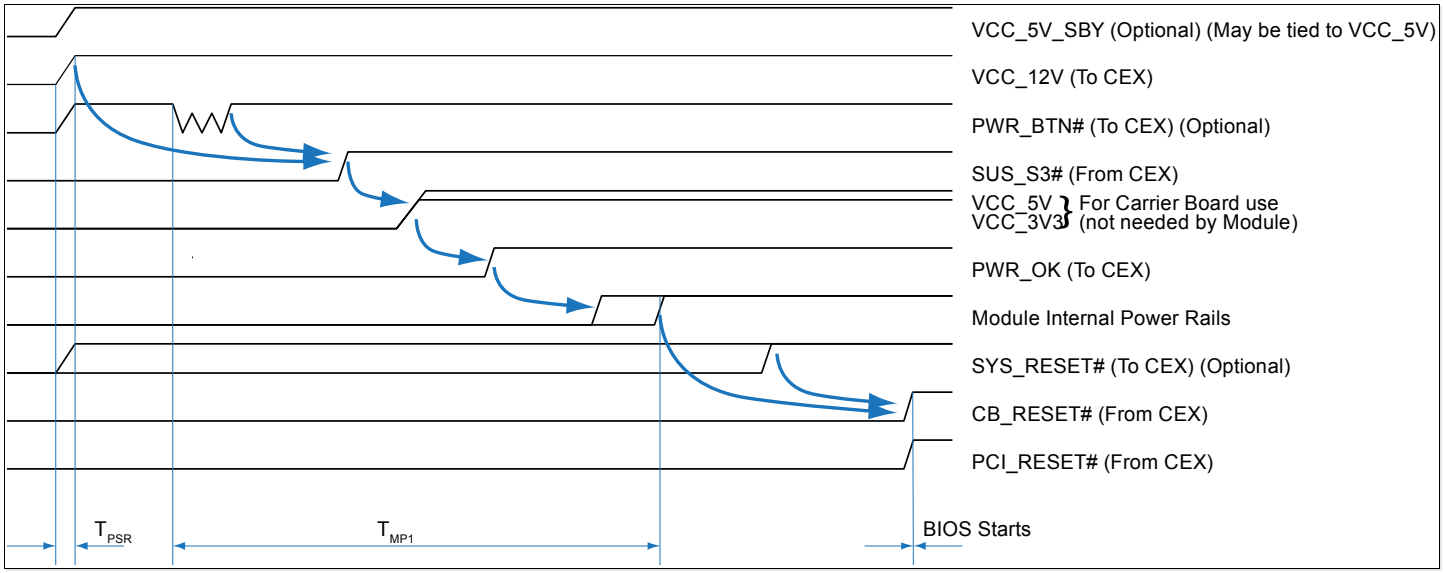


Figure 16 Carrier Power Sequence under AT Mode

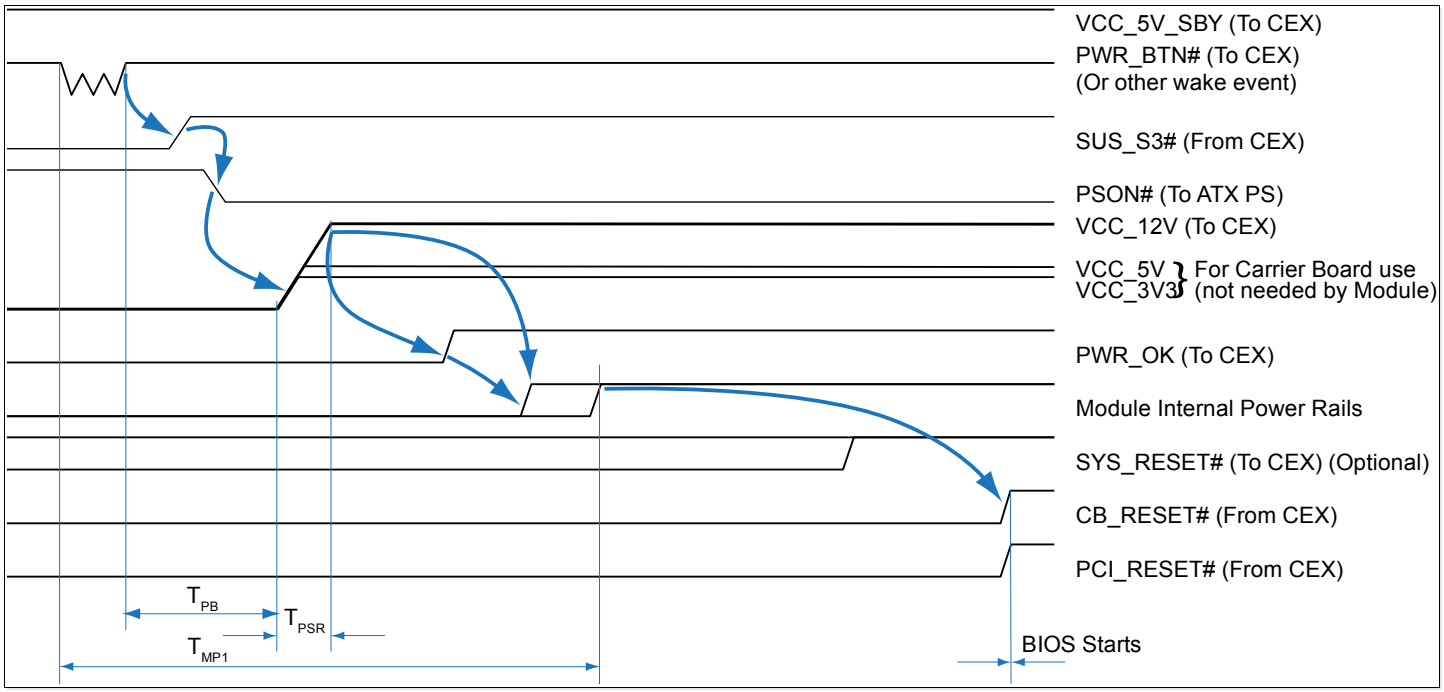


Figure 17 Carrier Power Sequence under ATX Mode

5 Mechanical

5.1 PCOM-B700G-NS Dimension

PCOM-B700G-NS top side view dimension

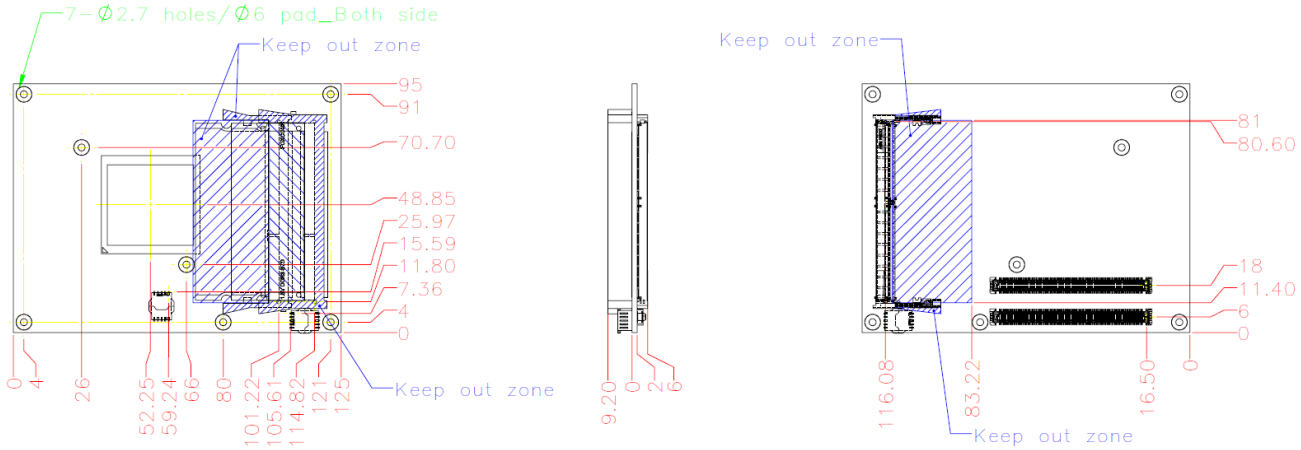


Figure 18 PCOM-B700G-NS Dimension – TOP & Bottom

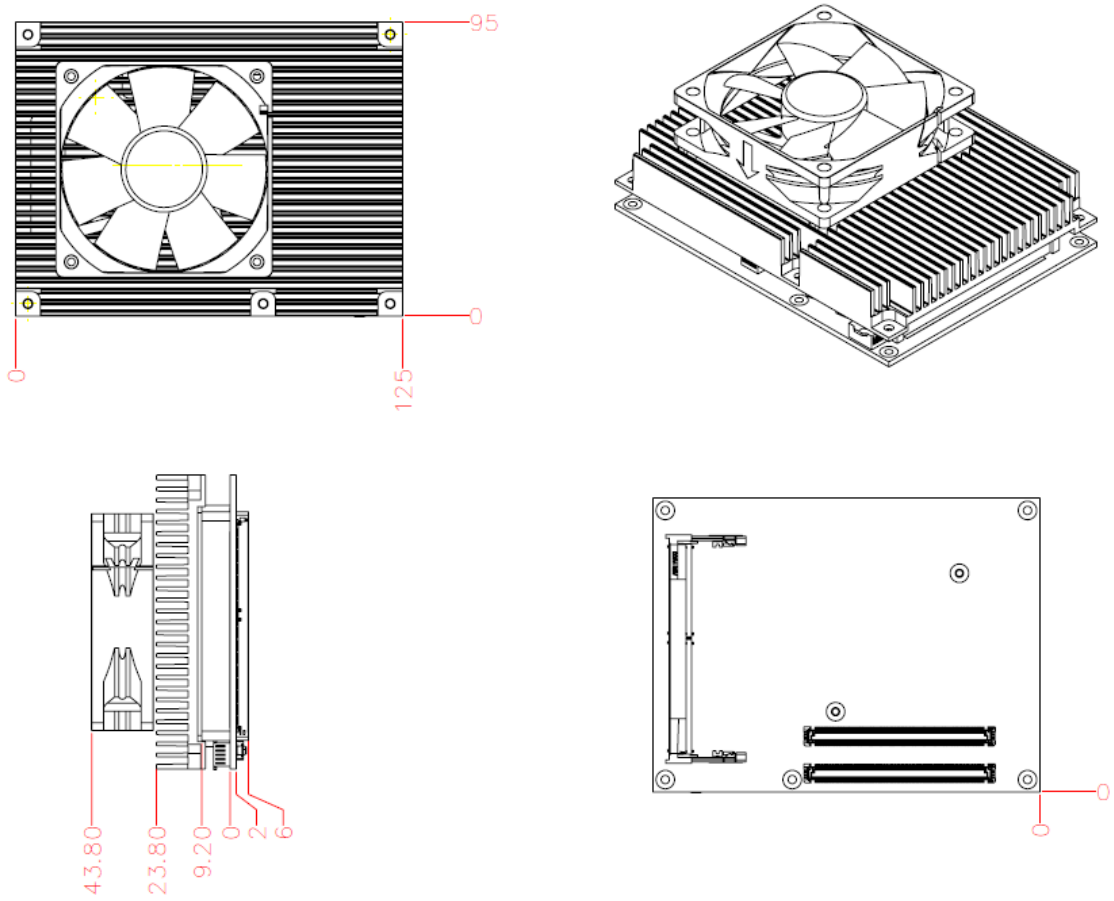


Figure 19 PCOM-B700G-NS side view dimension, along with a heat sink / cooler.

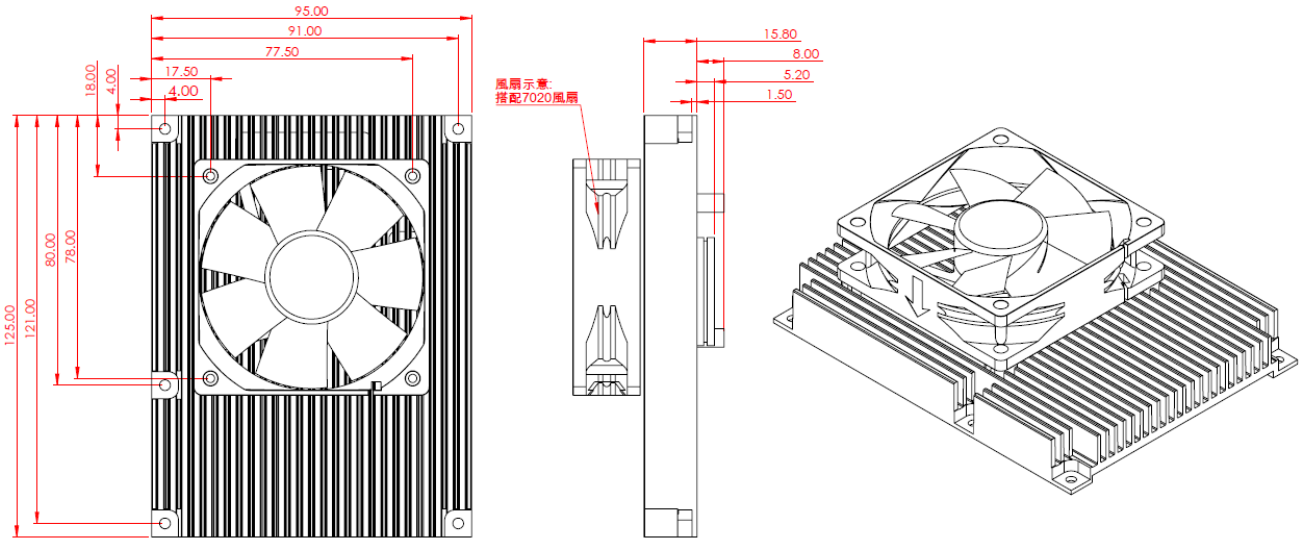


Figure 20 PCOM-B700G-NS Dimension - Side view

6 COM Express Module and Carrier protection design

6.1 Module protection

PCOM-B700G-NS Type 7, Schottky diode protection has been design on the COM Express module for Serial Port, FAN(PWMOUT & TACHIN), LID and SLEEP. Please refer to Fig.21 Module circuit protection schematic.

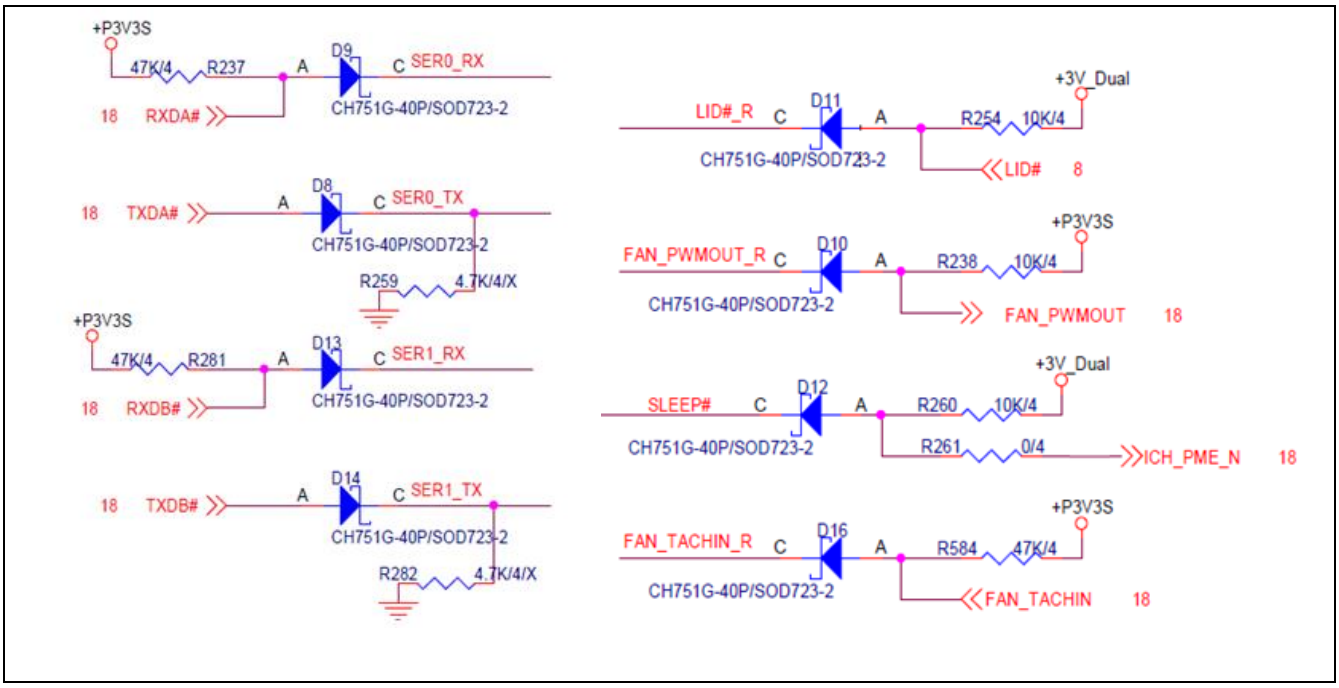


Figure 21 Circuit protection on Module

6.2 Carrier protection

Avoiding Carrier accidentally exposure to VCC_12V pool, a circuit protection design should be implemented on the Carrier, please refer to Fig.22 Carrier circuit protection schematic.

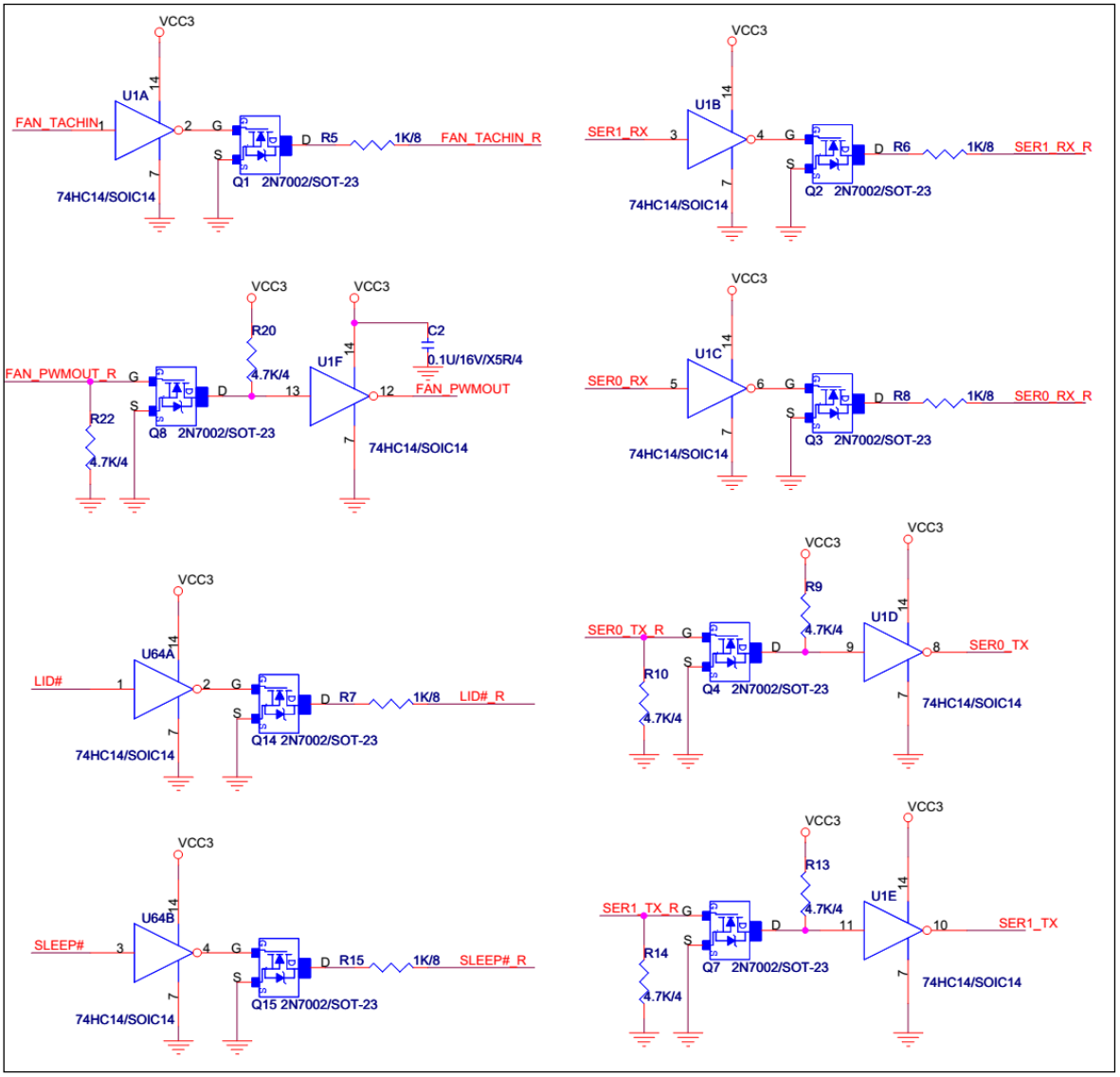


Figure 22 Circuit protection on Carrier

7 Industry Specifications

Low Pin Count Interface Specification, Revision 1.0 (LPC)
http://www.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0 http://www.usb.org/home
PCI Specification, Revision 2.3 https://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0 http://www.serialata.org/
PCI Express Base Specification, Revision 2.0 https://www.pcisig.com/specifications
PICMG® COM Express Module™ Base Specification http://www.picmg.org/
PICMG®COM Express Carrier Board Design Guide http://www.picmg.org/