



# Mobile Intel<sup>®</sup> 915GM/PM/GMS and 910GML Express Chipset

Specification Update

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*June 2005*

**Notice:** The Mobile Intel<sup>®</sup> 915GM/PM/GMS and 910GML Express chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 307167-003



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The Intel® 915GM/PM/GMS and 910GML Express chipsets may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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# Revision History

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Revision	Description	Date
-001	Initial public release	March 2005
-002	<ul style="list-style-type: none"> <li>• Added Errata 25 – 27</li> <li>• Added Specification Change 2 – 5</li> <li>• Added Specification Clarification 1</li> <li>• Added Documentation Change 5</li> </ul>	May 2005
-003	<ul style="list-style-type: none"> <li>• Added Errata 28</li> <li>• Added Errata and Component Marking Information for C1 Stepping</li> </ul>	June 2005

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# Preface

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This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

## Affected Documents

Document Title	Document Location/Number
<i>Intel® 915GM/GMS/PM and 910GML Express Chipset Datasheet</i>	<a href="#">305264</a>

## Nomenclature

**Errata** are design defects or errors. Errata may cause the behavior of the Intel® 915GM/PM/GMS and 910GML Express chipset GMCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

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## Summary Tables of Changes

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The following table indicates the Errata, Specification Changes, Specification Clarifications or Documentation Changes which apply to the listed Intel 915GM/PM/GMS and 910GML Express Chipset GMCH steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

### Codes Used in Summary Tables

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This item is either new or modified from the previous version of the document.

No	Steppings								Plans	ERRATA
	915PM		915GM		915GMS		910GML			
	C0	C1	B1	C1	C0	C1	B1	C1		
1	X	X	X	X					No Fix	Reported L0s exit latency is not updated when PCI Express* is not operating in Common Clock mode
2	X	X	X	X					No Fix	GMCH will not identify back to back malformed packets.
3	X	X	X	X					No Fix	The GMCH is limited to reporting Poisoned TLPs through standard PCI error status reporting structures
4	X	X	X	X					No Fix	Incorrect PCI Express Lane transition after receiving several TS1 packets.
5	X	X	X	X	X	X	X	X	No Fix	DMI Link Egress port address is not programmable
6	X	X	X	X	X	X	X	X	No Fix	DDR2 OCD nonfunctional
7	X	X	X	X	X				No Fix	PCI Express Graphics initiated snooped reads to memory that are fast dispatched could result in incorrect data being returned
8	X	X	X	X	X				No Fix	PCI Express common mode voltage noise immediately following Receiver Detect sequence
9	X	X	X	X	X				No Fix	GMCH does not ignore a PCI Express Null Packet
10	X	X	X	X	X				No Fix	Data payload byte count supplied during an unsupported upstream configuration read is not 4 bytes
11	X	X	X	X	X				No Fix	PCI Express Replay Timer Register default setting is incorrect
12	X	X	X	X	X	X	X	X	No Fix	E_SMERR bit set incorrectly
13			X						Fixed	PCI Express lane 3 bit errors occur on a small percentage of GMCH B-1 units on certain boards. PCI Express x16 interface only supported on C0 or later stepping.
14			X	X	X	X	X	X	No Fix	Pixel discoloration seen when Intel® Dual Frequency GraphicsTechnology (DFGT) is enabled
15	X		X		X		X		Fixed	System Hang with DDR-333 memory when Intel® Rapid Memory Power Management is enabled during C2/C3/C4
16			X		X				Fixed	Display becomes a solid color with Intel® S2DDT enabled (Only supported on 915GM & 915GMS)
17	X	X	X	X					No Fix	PCI Express Scrambling
18			X		X		X		Fixed	Macrovision Failue for 480p / 576p modes





No	Steppings								Plans	ERRATA
	915PM		915GM		915GMS		910GML			
	C0	C1	B1	C1	C0	C1	B1	C1		
19	X	X	X	X	X	X	X	X	No Fix	Thermometer Read Register is Non-Functional with Negative calibration offset
20	X	X	X	X	X	X	X	X	No Fix	Potential electrical spec violation if a SO-DIMM is only populated in Channel B
21			X	X	X	X	X	X	No Fix	LVDS Panel power down timing violation during system reset
22	X	X	X	X					No Fix	PCI Express SKP/InitFCx Contention Erratum
23	X		X		X		X		Fixed	SMVREF High Current Draw
24			X	X	X	X	X	X	No Fix	Mobile Intel® 915GM/GMS and 910GML Graphics Clock Crossing issue
25	X	X	X	X	X	X	X	X	NoFix	Mobile Intel® 915GM/PM/GMS and 910GML Express Chipset Memory Refresh Queue Erratum
26	X	X	X	X					NoFix	Packet Dropped When Replay Timer Expires and Replay is in Progress
27	X	X	X	X	X	X	X	X	NoFix	LOCK to non-DRAM Memory Flag (Register Dev 0, Fun 0, Offset C8, Bit 9) is Getting Asserted
28			X	X	X	X	X	X	NoFix	Mobile Intel® 915GM/GMS and 910GML Express Chipset LVDS ↔ CRT Switching Erratum

Number	SPECIFICATION CHANGES
1	Graphics Render and Display Clock Frequency Combination Support
2	Intel® 915GM Host/Memory/Graphics Clock Support Update
3	Intel® 915GM Host/Memory/Graphics Clock Support Table 11-1 Update
4	Mobile Intel® 915GM/GMS and 910GML Express Chipset Display and Render clock support updates
5	Mobile Intel® 910GML Express Chipset Memory Channel Organization Support update

Number	SPECIFICATION CLARIFICATIONS
1	Slow Transfers for LPC Devices

Number	DOCUMENTATION CHANGES
1	DRAM Enhanced Addressing Update
2	Section 5.2.15 C0DRC1 – Channel 0 DRAM Controller Mode 1
3	Section 5.2.31 DCC – DRAM Channel Control
4	Section 2.2.33 GCFG – Graphics Clock Frequency and Gating Control
5	Section 5.2.12 C0DRT1 – Channel 0 DRAM Timing Register 1

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# Identification Information

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## Component Identification via Programming Interface

The Intel® 915GM/PM/GMS and 910GML Express chipset family may be identified by the following register contents:

Stepping	Vendor ID <sup>1</sup>	Device ID <sup>2</sup>	Revision Number <sup>3</sup>
B1	8086h	2590h	03
C0	8086h	2590h	03

**NOTES:**

1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration spaces.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration spaces.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration spaces.

## Component Marking Information

The Intel 915GM/PM/GMS and 910GML Express chipset family may be identified by the following component markings:

Product	MM#	Stepping	Notes
Mobile Intel® 915GM Express Chipset	865926	B1	
Mobile Intel® 915GM Express Chipset	865971	B1	Pb-free
Mobile Intel® 910GML Express Chipset	865930	B1	
Mobile Intel® 910GML Express Chipset	865923	B1	Pb-free
Mobile Intel® 915PM Express Chipset	867706	C0	
Mobile Intel® 915PM Express Chipset	867713	C0	Pb-free
Mobile Intel® 915GMS Express Chipset	867708	C0	
Mobile Intel® 915GMS Express Chipset	867712	C0	Pb-free
Mobile Intel 915 GM Express Chipset	SL8G2	C1	
Mobile Intel 915 GM Express Chipset	SL8G6	C1	Pb-free
Mobile Intel 915 PM Express Chipset	SL8G3	C1	
Mobile Intel 915 PM Express Chipset	SL8G7	C1	Pb-free
Mobile Intel 915 GMS Express Chipset	SL8G4	C1	
Mobile Intel 915 GMS Express Chipset	SL8G8	C1	Pb-free
Mobile Intel 910 GML Express Chipset	SL8G5	C1	
Mobile Intel 910 GML Express Chipset	SL8G9	C1	Pb-free

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## Errata

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### 1. **Reported L0s Exit Latency Is Not Updated When PCI Express\* Is Not Operating in Common Clock Mode**

**Problem:** When PCI Express is operating with separate reference clocks, L0s exit latency may be greater than the setting in the L0s Exit Latency register.

**Implication:** If the PCI Express link is operating in non-common clock mode, the actual L0s exit latency may be longer than advertised. In this situation the link will likely enter the Recovery state before transitioning into the normal L0 state.

**Workaround:** System BIOS can program the appropriate Exit Latency and advertised N\_FTS value if it detects that the downstream device is not using the common reference clock (indicated in the Slot Clock Configuration bit 12 of the device's Link Status register).

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

### 2. **GMCH Will Not Identify Back-to-Back Malformed Packets**

**Problem:** If the GMCH receives two back-to-back malformed packets, the second malformed packet is not trapped or logged.

**Implication:** The GMCH will not log or identify the second malformed packet. However, the 1<sup>st</sup> malformed TLP is logged, and is considered a Fatal Error. Link behavior is not guaranteed at that point whether a 2<sup>nd</sup> malformed TLP is detected or not.

**Workaround:** None

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

### 3. **The GMCH Is Limited to Reporting Poisoned TLPs through Standard PCI Error Status Reporting Structures**

**Problem:** The GMCH does not set the Non-Fatal Error Detected status bit, in the PCI Express Device Status register when a poisoned TLP is received.

**Implication:** Future OS's (that comprehend PCI Express error reporting) will not be notified via standard PCI Express mechanisms when a poisoned TLP is received.

**Workaround:** Standard PCI error status reporting must be used for Poisoned TLP reporting. The reception of Poisoned TLP is reported by hardware setting the Detected Parity Error bit in Device 1, secondary status register, and if so enabled by additionally setting the Master Data Parity Error bit in the same register.

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

#### 4. **Incorrect PCI Express\* Lane Transition after Receiving Several TS1 Packets**

**Problem:** If the GMCH receives several TS1 packets with Link and Lane numbers set to PAD, after 4  $\mu$ s it will time out and transition into configuration state instead of going directly to the Detect state as it should. However, the link will still transition to the Detect state after timing out of Configuration.

**Implication:** The GMCH will experience longer latency when transitioning to Detect state.

**Workaround:** None

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

#### 5. **DMI Link Egress Port Address Is Not Programmable**

**Problem:** The PCI SIG approved ECR 04 to allow future system software (e.g., operating system) to discover the link structure of the Root Complex. One of the registers in the GMCH that “points” from the DMI port to the ICH cannot be programmed correctly.

**Implication:** There is no impact on platform functionality. ECR’s do not retroactively apply to the current *PCI Express\* 1.0a Specification* and no existing software understands the Root Topology discovery structures. These structures are implemented in the GMCH only to aid future software development. Such software will need to comprehend the incorrect pointer

**Workaround:** None

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

#### 6. **DDR2 OCD Nonfunctional**

**Problem:** During BIOS initialization the GMCH will not be able to adjust and set the DDR2-DRAM Device DQ/DQS/DQS# buffer impedance.

**Implication:** Adjustable DQ/DQS/DQS# buffer impedance settings will not be programmed into the DDR2-DRAM Devices, and the DRAM device OCD default output characteristics will be used instead.

**Workaround:** None

**Status:** DDR2 OCD has been defeatured. For the steppings affected, see the *Summary Tables of Changes*.

#### 7. **PCI Express\* Graphics Initiated Snooped Reads to Memory That Are Fast Dispatched Could Result in Incorrect Data Being Returned**

**Problem:** This has only occurred at 1.05-V Core and 533-MHz FSB. GMCH could provide incorrect data for a PCI Express Graphics initiated memory read.

**Implication:** Could cause a data miscompare or system hang.

**Workaround:** Disable snooped reads being fast dispatched. This can be done by setting MCHBAR Offset 44h Bit[0] to "1". Will be included in BIOS Spec update version 0.54.

**Status:** For the steppings affected, see the *Summary Tables of Changes*.



## 8. PCI Express\* Common Mode Voltage Noise Immediately following Receiver Detect Sequence

**Problem:** The PCI Express Common Mode Voltage is not stable immediately after Receiver Detect Sequence when entering Polling.Active from Detect.Active states.

**Implication:** Common Mode Voltage noise may result in bit errors early in Polling.Active state. May result in additional training time before transitioning on to Polling.Configuration. Performance impact expected to be minimal.

**Workaround:** None

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

## 9. GMCH Does Not Ignore a PCI Express\* Null Packet

**Problem:** If the GMCH receives a PCI Express Null packet, it should drop the packet and not perform sequence number checking or respond with any Ack or Nak DLLP. The issue is that the GMCH still performs sequence number checks for Null packets and may respond with an ACK or NAK depending on the result of the check.

**Implication:** GMCH may send ACK or NAK DLLPs in response to a Null packet if the sequence number is not as expected. This may cause unnecessary retries, but Null packets are expected to be rare on the link.

**Workaround:** None

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

## 10. Data Payload Byte Count Supplied during an Unsupported Upstream Configuration Read Is Not 4 Bytes

**Problem:** During configuration reads to unsupported PCI Express configuration space, the byte count for data payload is not 4.

**Implication:** Data payload byte count is 5 and not the expected 4.

**Workaround:** Do not perform unsupported upstream PCI Express configuration cycles.

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

## 11. PCI Express Replay Timer Register Default Setting Is Incorrect

**Problem:** The default Replay timer value is too aggressive and does not properly account for L0s exit latency or internal pipeline delays. As a result the GMCH may initiate a replay sooner than expected.

**Implication:** The GMCH may initiate a replay sooner than expected. This should not happen as long as the downstream device complies with the PCI Express Ack Latency requirement.

**Workaround:** **It is possible for BIOS to contain a workaround. Contact your Intel Field Rep for more details**

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

## 12. **E\_SMERR Bit Set Incorrectly**

**Problem:** The E\_SMERR bit may be incorrectly set when performing valid accesses to SMM space.

**Implication:** If this bit is used by the SMI handler to determine cache line flushes, unnecessary cache line flushes may occur when in SMM mode. A slight performance impact to the SMI handler may result from unnecessary cache line flushes.

**Workaround:** None

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

## 13. **PCI Express\* Lane 3 Bit Errors Occur on a Small Percentage of GMCH B-1 Units on Certain Boards**

**Problem:** On systems with External Graphics, a small percentage of GMCH B-1 units may experience bit-errors on PCI Express lane 3 on certain boards. To date, we have only seen these bit errors on internal test (SV) boards at nominal core voltage (1.05 V).

**Implication:** A significant level of bit errors could lead to link retraining, link down, or hang conditions. Intel is currently trying to understand the variables that affect the bit error rate. All samples shipped outside of Intel have been screened for this issue and Intel has not seen any system hangs with screened parts. *PCI Express x16 Graphics not supported on Mobile Intel 915GM B1 stepping.*

**Workaround:** None

**Status:** For affected steppings, see the *Summary Tables of Changes*.

## 14. **Pixel Discoloration Seen When Intel® Dual Frequency Graphics Technology (DFGT) Is Enabled**

**Problem:** Pixel discoloration seen when Intel Dual Frequency Graphics Technology (DFGT) is enabled. Root caused to the internal render clocks getting misaligned during the frequency switching.

**Implication:** Pixel discoloration seen on display.

**Workaround:** Disable the DFGT feature through VBT.

**Status:** For affected steppings, see the *Summary Table of Changes*.

## 15. **System Hang with DDR-333 Memory When Intel® Rapid Memory Power Management Is Enabled During C2/C3/C4**

**Problem:** DDR333 systems may not exit self refresh state when memory self refresh is enabled during C2/C3/C4.

**Implication:** System may hang.

**Workaround:** None.

**Status:** Disable Intel Rapid Memory Power Management in systems with DDR memory for affected steppings. For the steppings affected, see the *Summary Tables of Changes*.





## 16. Display becomes a Solid Color with Intel® S2DDT Enabled

**Problem:** If Memory Self-Refresh during C3 (C3SR) occurs when the Smart 2D Display Technology (S2DDT) recompresses at the start of a frame, the graphics engine may use the uncompressed frame instead of the recompressed frame. The issue may occur if the system is left idle (>20 minutes) with S2DDT.

**Implication:** Display becomes a solid color or may cause a system hang.

**Workaround:** None

**Status:** Intel S2DDT is disabled in production graphics driver for affected stepping. For the steppings affected, see the *Summary Tables of Changes*.

## 17. PCI Express Scrambling

**Problem:** While entering the Recovery state, 915GM/PM PCI Express discrete graphics port stops scrambling two symbols before the first TS (training sequence).

**Implication:** When these non-scrambled symbols are received by the endpoint, the de-scrambler of the endpoint will observe two symbols of random data. The first symbol of TS1 will reset the endpoint's de-scrambler so that the endpoint should recognize the TS1 and TS2 ordered-sets being transmitted and move into the Recovery state as planned. There is no system level impact if the endpoint is PCI Express Specification 1.0a compliant in ignoring the random data.

**Workaround:** None

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

## 18. Macrovision Failure for 480p / 576p Modes

**Problem:** GMCH does not encode Macrovision (content protection) properly for 480p and 578p progressive modes and does not meet the Macrovision specification for these modes. 480p and 576p progressive modes will not pass MacroVision certification.

**Implication:** No DVD playback supported/available for these modes, other progressive scan modes are not affected.

**Workaround:** None

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

## 19. Thermometer Read Register is Non-Functional with Negative Calibration Offset

**Problem:** When initializing the Thermometer counter, a negative offset will cause an overflow condition, causing the counter to stop. The GMCH will not update the Thermometer Read Register (TRR) register with the correct temperature trending values and the TRR will display "FF". All other thermal sensor features will still work (throttling, trip points and interrupts) since these do not use the thermometer mode.

**Implication:** Thermometer Read Register (TRR) is not functional with negative Thermal Calibration Offset value (TCO).

**Workaround:** Please contact your Intel representative for the latest information.

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

## 20. Potential Electrical Spec Violation if an SO-DIMM Is Only Populated in Channel B

- Problem:** When DDR or DDR2 memory devices are present on channel B, but not channel A, memory control logic only looks at channel A and incorrectly performs Rcomp value update. This could cause an electrical spec violation internal to the chip.
- Implication:** System with 915GM/PM/GML may hang or experience other anomalous system behavior. No impact on system with 915GMS.
- Workaround:** **It is possible for BIOS to contain a workaround. Contact your Intel Field Rep for more details**
- Status:** For the steppings affected, see the *Summary Tables of Changes*.

## 21. LVDS Panel Power Down Timing Violation during System Reset

- Problem:** During system reset, there is insufficient time for handshake between ICH and GMCH LVDS logic. As a result, timing from panel backlight enable going low to LVDS data going low (TX) and timing from LVDS data going low to panel VCC enable going low (T3) do not match the programmed values. Panel backlight enable (LBKLT\_EN), panel Vcc enable (LVDD\_EN) and LVDS data lines go low at the same time.
- Implication:** No system level issues have been observed.
- Workaround:** None
- Status:** For the steppings affected, see the *Summary Tables of Changes*.

## 22. PCI Express SKP/InitFCx Contention

- Problem:** During GMCH PCI Express initialization, if a SKP is being transmitted immediately before an InitFCx DLLP, then a partial InitFCx may be transmitted.
- Implication:** A slight delay (less than 100 ns) may occur during link initialization. Device may report correctable error. InitFCx will automatically be repeated.
- Workaround:** None
- Status:** For the steppings affected, see the *Summary Tables of Changes*

## 23. SMVREF High Current Draw

- Problem:** When SMOCDCOMP[1:0] are connected to ground (either directly or through a pull-down resistor), SMVREF[1:0] may draw significantly more current than specified. If the corresponding voltage supply is not capable of handling the resulting current, the SMVREF[1:0] voltage will droop below specification.
- Implication:** If SMVREF[1:0] droops below specification, the system may hang. Failure observed during S3 only.
- Workaround:** Leave SMOCDCOMP[1:0] as NC (No Connect) for both DDR and DDR2 designs. This limits the maximum current draw on SMVREF[1:0] to 200  $\mu$ A (i.e. 100 $\mu$ A/pin). In addition, use a voltage supply that can supply at least 200  $\mu$ A (total) for SMVREF[1:0].
- Status:** For the steppings affected, see the *Summary Tables of Changes*.



## 24. Mobile Intel® 915GM/GMS and 910GML Graphics Clock Crossing issue

**Problem:** While attempting to launch or exit an application that uses the overlay engine (e.g. media playback software running a video clip), the system may hang (blue screen) or screen resolution may change to VGA mode. This event may occur when a signal pulse is missed inside the chip due to synchronization of the graphics render and display clocks while graphics overlay mode is being turned off.

**Implication:** Failure is difficult to reproduce because this event only occurs under a very rare but valid timing condition where graphics render and display clocks are aligned while the graphics overlay is being turned off. System will hang or screen resolution may change to VGA mode when launching or exiting an application that uses the overlay engine. Mobile Intel 915GM/GMS and 910GML platforms that use render clock at 166 MHz are not affected by this sighting.

**Workaround:** It is possible for BIOS to contain a workaround. Contact your Intel Field Representative for more details.

**Status:** For the steppings affected, see the *Summary Tables of Changes*.

## 25. Mobile Intel® 915GM/PM/GMS and 910GML Express Chipset Memory Refresh Queue Erratum

**Problem:** When thermal based throttling is enabled, memory refresh commands get queued up inside MCH/GMCH. As a result, MCH/GMCH may not perform memory refresh commands at a frequency needed by memory devices. Thermal based throttling happens only when either using the on-die memory thermal sensors or the external thermal sensor.

**Implication:** When not enough refresh commands are issued to system memory to retain memory content, data loss may occur. System is more susceptible to this issue when memory devices approach temperature limit.

**Workaround:** Prioritize memory refresh commands via BIOS changes:

- MCHBAR Offset 164h bit 15 = 1 for Channel A memory
- MCHBAR Offset 1E4h bit 15 – 1 for Channel B memory

**Status:** BIOS fix available (required only for thermal based throttling). Please refer to BIOS Spec update Rev 1.92 for more details. For affected steppings, see the *Summary Tables of Changes*.

## 26. Packet Dropped When Replay Timer Expires and Replay Is in Progress

**Problem:** When a packet replay is in progress on the PCI Express\* Port, and if some but not all of the packets to be replayed are acknowledged and the replay timer expires on the same clock cycle as the replay start of the first unacknowledged packet, the next packet in the replay buffer may be sent with an old sequence number. That packet is seen by receiver side as a duplicate and subsequently dropped.

Note: This has only been reproduced in a synthetic test environment.

**Implication:** Anomalous behavior may result if all of the above conditions are met.

**Workaround:** None

**Status:** No plan to fix. For affected steppings, see the *Summary Tables of Changes*.

## 27. LOCK to non-DRAM Memory Flag (Register Dev 0, Fun 0, Offset C8, Bit 9) Is Getting Asserted

**Problem:** A CPU lock cycle request is unintentionally being recognized as request to a non-system memory destination.

**Implication:** The GMCH may incorrectly flag an error for a valid lock cycle that targets DRAM. A System Error (SERR) may be generated if enabled by System BIOS.

Note: The default setting for ERRCMD[9] Bus 0 Device 0 Offset CAh is to disable this reporting.

**Workaround:** Do not enable or change default setting of ERRCMD[9] Bus 0 Device 0 Offset CAh (SERR reporting for Lock cycles to non-DRAM Memory)

**Status:** For affected steppings, see the *Summary Tables of Changes*.

## 28. Mobile Intel® 915GM/GMS and 910GML Express Chipset LVDS – CRT Switching Erratum

**Problem:** 915GM/GMS and 910GML LVDS interface may hang while switching between LVDS and CRT outputs.

**Implication:** Once LVDS interface hangs a system reset is required.

**Workaround:** Fixed in VBIOS, Please refer to release notes for VBIOS version 1220 or Newer.

**Status:** For affected steppings, see the *Summary Tables of Changes*.

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# Specification Changes

## 1. Graphics Core Clock Frequency Update

The following section replaces the *Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet*, Section 10.14.3.

### 10.14.3.1 Intel® 915GM Host/Memory/Graphics Clock Support

**Table 10-16a. Intel® 915GM Graphics Clock Frequency Support at 1.05 V**

Host	Memory	2D Display clock	3D Render Clock
400 MHz	DDR 333	200	166
400 MHz	DDR 333	213	200
533 MHz	DDR 333	190	166
533 MHz	DDR 333	213	190
400 MHz / 533 MHz	DDR2 400 / DDR2 533	200	160
400 MHz / 533 MHz	DDR2 400 / DDR2 533	213	200

**NOTE:** Mobile Intel 915GM / 910GML will remove support for 133 MHz for both graphics render and display clock due to graphics clock crossing issue (Errata #24).

**Table 10-16b. Intel® 915GM Graphics Clock Frequency Support at 1.5 V**

Host	Memory	2D Display clock	3D Render Clock
400 MHz / 533 MHz	DDR2 400 / DDR2 533	200	160
400 MHz / 533 MHz	DDR2 400 / DDR2 533	213	200
400 MHz / 533 MHz	DDR2 400 / DDR2 533	333	333

**NOTE:** Mobile Intel 915GM / 910GML does not support DDR333 if chipset core voltage is designed for 1.5 V.

### 10.14.3.2 Intel® 915GMS Host/Memory/Graphics Clock Support

**Table 10-17. Intel® 915GMS Graphics Clock Frequency Support at 1.05 V**

Host	Memory	2D Display clock	3D Render Clock
400 MHz	DDR2 400	152	133
400 MHz	DDR2 400	200	160

### 10.14.3.3 Intel® 910GML Host/Memory/Graphics Clock Support

**Table 10-18. Intel® 910GML Graphics Clock Frequency Support at 1.05 V**

Host	Memory	2D Display clock	3D Render Clock
400 MHz	DDR 333	200	166
400 MHz	DDR2 400	200	160

## 2. Intel® 915GM Host/Memory/Graphics Clock Support Update

Table 10-16 and Table 10-7 incorrectly state support for Display clocks for 400 MHz / DDR333 and 533 MHz/DDR333 frequency combinations. These combinations will result with a Display clock of 222 MHz. See Specification Change Item #1 above and Documentation Change #4 for updated information in grey shaded text.

## 3. Mobile Intel® 915GM/GMS and 910GML Express Chipset Display and Render Clock Support Update

The following section replaces the *Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet, Graphics Clock Frequency Feature* section, on page 22.

- 2D Display core frequency at 190/200 or 213/222 MHz @ Vcc=1.05 V depending on the host/memory configurations
- 3D Render core frequency at 160/166 or 190/200 MHz @ Vcc=1.05 V depending on the host/memory configurations
- 2D Display core frequency at 200, 213 or 333 MHz @ Vcc=1.5 V depending on the host/memory configurations
- 3D Render core frequency at 166, 200 or 333 MHz @ Vcc=1.5 V depending on the host/memory configurations

The following section replaces the *Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet, Graphics Clock Frequency Feature* section, on page 25.

- 2D Display core frequency at 152 or 200 MHz @ Vcc=1.05 V depending on the host/memory configurations
- 3D Render core frequency at 133 or 160 MHz @ Vcc=1.05 V depending on the host/memory configurations



The following section replaces the *Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet, Graphics Clock Frequency Feature* section, on page 26.

- 2D Display core frequency at 200 MHz @ Vcc=1.05 V depending on the host/memory configurations
- 3D Render core frequency at 160/166 MHz @ Vcc=1.05 V depending on the host/memory configurations

#### 4. **Mobile Intel® 910GML Express Chipset Memory Channel Organization Support Update**

The following section replaces the *Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet* in the *Mobile Intel 910GML Express Chipset Feature* section, on page 26 and in Section 10.2.

- Memory channel organization support for DDR is:
    - Single Channel Mode
  - Memory channel organization support for DDR2 is:
    - Dual Channel Asymmetric Mode only
- Note:** Dual Channel Symmetric (Interleave) Mode not supported on Mobile Intel 910GML Express chipset

The following bullet replaces the *Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet, Section 10.2, System Memory Controller*.

- Dual Channel Symmetric (Interleave) Mode not supported for Mobile Intel 910GML Express chipset.

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# Specification Clarifications

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## 1. **Slow DMA Transfers for LPC Devices**

8-bit DMA transfers to some LPC devices, may incur latencies, that result in a slowed down transfer rate. Longer latencies may occur when the platform becomes idle and the GMCH dynamically asserts HCPUSLP# for Processor C2 states.

For example, A 4-Mbps FIR device may transmit faster than the resulting 8-bit DMA transfer rate resulting in data retransmission and lower FIR throughput.

So as not to impede the transfer rate of certain LPC Devices, the dynamic assertion of HCPUSLP# by GMCH during Processor C2 states can be disabled. See BIOS Spec Update 1.93 for details on how to disable HCPUSLP# assertion during C2 states.

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# Documentation Changes

## 1. DRAM Enhanced Addressing Update

The following section is inserted into the Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet Chapter 10, Section 10.2.1.3

### 10.2.1.3 DRAM Address Mapping

Enhanced Addressing swaps the most significant bit controlling one of the S<sub>x</sub>\_BS lines with bit 18 (which normally controls row address bit 2). Without Enhanced Addressing, rank bits are the most significant two bits of the address. With Enhanced Addressing, the rank bits are always bits 19 and 20.

**Table 10-8 DRAM Device Configurations – Dual Channel Asymmetric Mode w/Enh. Addr. Swap (0)**

<b>Technology (Mb)</b>	256	256	512	512	512	512	1024	1024	1024	1024
<b>Row bits</b>	13	13	13	13	13	14	14	14	13	14
<b>Column bits</b>	9	10	10	11	10	10	10	11	10	10
<b>Bank bits</b>	2	2	2	2	2	2	2	2	3	3
<b>Width (b)</b>	16	8	16	8	16	8	16	8	16	8
<b>Rows</b>	8192	8192	8192	8192	8192	16384	16384	16384	8192	16384
<b>Columns</b>	512	1024	1024	2048	1024	1024	1024	2048	1024	1024
<b>Banks</b>	4	4	4	4	4	4	4	4	8	8
<b>Page Size (KB)</b>	4	8	8	16	8	8	8	16	8	8
<b>Devices per rank</b>	4	8	4	8	4	8	4	8	4	8
<b>Rank Size (MB)</b>	128	256	256	512	256	512	512	1024	512	1024
<b>Depth (M)</b>	16	32	32	64	32	64	64	128	64	128
<b>Addr bits [n:0]</b>	26	27	27	28	27	28	28	29	28	29
<b>Available in DDR</b>	yes	yes	yes	yes	no	no	yes	yes	no	no
<b>Available in DDRII</b>	yes	yes	no	no	yes	yes	no	No	yes	yes
<b>Host Address bit</b>	<b>Mem Addr-bit</b>									
<b>31</b>	-	-	-	-	-	-	-	-	-	-
<b>30</b>	-	-	-	-	-	-	-	r 3	-	r 3
<b>29</b>	-	-	-	r 3	-	r 3	r 3	r 13	r 3	r 13
<b>28</b>	-	r 3	r 3	r 11	r 3	r 13	r 13	r 11	r 11	r 11
<b>27</b>	r 3	r 12	r 12	r 12	r 12	r 12	r 12	r 12	r 12	r 12
<b>26</b>	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10
<b>25</b>	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9

24	r8	r8	r8	r8	r8	r8	r8	r8	r8	r8
23	r7	r7	r7	r7	r7	r7	r7	r7	r7	r7
22	r6	r6	r6	r6	r6	r6	r6	r6	r6	r6
21	r5	r5	r5	r5	r5	r5	r5	r5	b2	b2
20	r4	r4	r4	r4	r4	r4	r4	r4	r4	r4
19	s0	s0	s0	s0	s0	s0	s0	s0	s0	s0
18	b1	b1	b1	b1	b1	b1	b1	b1	b1	b1
17	r1	r1	r1	r1	r1	r1	r1	r1	r1	r1
16	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0
15	r11	r11	r11	r2	r11	r11	r11	r2	r5	r5
14	r12	r2	r2	b0	r2	r2	r2	b0	r2	r2
13	r2	b0	b0	c11	b0	b0	b0	c11	b0	b0
12	b0	c9	c9	c9	c9	c9	c9	c9	c9	c9
11	c8	c8	c8	c8	c8	c8	c8	c8	c8	c8
10	c7	c7	c7	c7	c7	c7	c7	c7	c7	c7
9	c6	c6	c6	c6	c6	c6	c6	c6	c6	c6
8	c5	c5	c5	c5	c5	c5	c5	c5	c5	c5
7	c4	c4	c4	c4	c4	c4	c4	c4	c4	c4
6	c3	c3	c3	c3	c3	c3	c3	c3	c3	c3
5	c2	c2	c2	c2	c2	c2	c2	c2	c2	c2
4	c1	c1	c1	c1	c1	c1	c1	c1	c1	c1
3	c0	c0	c0	c0	c0	c0	c0	c0	c0	c0



**Table 10-9 DRAM Device Configurations –Dual Channel Interleaved Mode w/ Enh. Addr. Swap (0)**

<b>Technology (Mb)</b>	256	256	512	512	512	512	1024	1024	1024	1024
<b>Row bits</b>	13	13	13	13	13	14	14	14	13	14
<b>Column bits</b>	9	10	10	11	10	10	10	11	10	10
<b>Bank bits</b>	2	2	2	2	2	2	2	2	3	3
<b>Width (b)</b>	16	8	16	8	16	8	16	8	16	8
<b>Rows</b>	8192	8192	8192	8192	8192	16384	16384	16384	8192	16384
<b>Columns</b>	512	1024	1024	2048	1024	1024	1024	2048	1024	1024
<b>Banks</b>	4	4	4	4	4	4	4	4	8	8
<b>Page Size (KB)</b>	4	8	8	16	8	8	8	16	8	8
<b>Devices per rank</b>	4	8	4	8	4	8	4	8	4	8
<b>Rank Size (MB)</b>	128	256	256	512	256	512	512	1024	512	1024
<b>Depth (M)</b>	16	32	32	64	32	64	64	128	64	128
<b>Addr bits [n:0]</b>	26	27	27	28	27	28	28	29	28	29
<b>Available in DDR</b>	yes	yes	yes	yes	no	no	yes	Yes	no	no
<b>Available in DDRII</b>	yes	yes	no	no	yes	yes	no	No	yes	yes
<b>Host Address bit</b>	<b>Mem Addr-bit</b>									
<b>31</b>	-	-	-	-	-	-	-	r 3	-	r 3
<b>30</b>	-	-	-	r 3	-	r 3	r 3	r 13	r 3	r 13
<b>29</b>	-	r 3	r 3	r 11	r 3	r 13	r 13	r 11	r 11	r 11
<b>28</b>	r 3	r 12	r 12	r 12	r 12	r 12	r 12	r 12	r 12	r 12
<b>27</b>	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10
<b>26</b>	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9
<b>25</b>	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8
<b>24</b>	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7
<b>23</b>	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6
<b>22</b>	r 5	r 5	r 5	r 5	r 5	r 5	r 5	r 5	b 2	b 2
<b>21</b>	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4
<b>20</b>	s 0	s 0	s 0	s 0	s 0	s 0	s 0	s 0	s 0	s 0
<b>19</b>	b 1	b 1	b 1	b 1	b 1	b 1	b 1	b 1	b 1	b 1
<b>18</b>	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1
<b>17</b>	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0
<b>16</b>	r 11	r 11	r 11	r 2	r 11	r 11	r 11	r 2	r 5	r 5
<b>15</b>	r 12	r 2	r 2	b 0	r 2	r 2	r 2	b 0	r 2	r 2
<b>14</b>	r 2	b 0	b 0	c 11	b 0	b 0	b 0	c 11	b 0	b 0
<b>13</b>	b 0	c 9	c 9	c 9	c 9	c 9	c 9	c 9	c 9	c 9
<b>12</b>	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8
<b>11</b>	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7
<b>10</b>	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6

9	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5
8	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4
7	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3
6	h	h	h	h	h	h	h	H	h	h
5	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2
4	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1
3	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0

## 2. Section 5.2.15 C0DRC1 – Channel 0 DRAM Controller Mode 1

The following register bits definition replaces the *Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet*, Section 5.2.15

### C0DRC1—Channel 0 DRAM Controller Mode 1

PCI Device: MCHBAR  
 Address Offset: 124h  
 Default Value: 00000000h  
 Access: RO, R/W  
 Size: 32 bits

Bit	Access and Default	Description
31	R/W 0 b	<b>Swap Mode Enable.</b> 0 = Swap mode disabled. Dram Address Map Follows the standard address map described in the EDS. 1 = Swap mode enabled. This bit can be enabled if all dimm are either single sided or symmetrically populated.
30	R/W 0 b	<b>Reserved</b>
29	R/W 00 b	<b>Address Swap Mode.</b> 0 = Swap Enabled for Bank Selects and Rank Selects. 1 = Swap Enabled for Bank Selects only.
28:27	RO 0 b	<b>Reserved</b>



Bit	Access and Default	Description																																																																								
26:24	R/W 000 b	<p><b>Swap Address Selection</b></p> <p><b>Single Channel and Asymm-Stacked Dual Channel:</b></p> <table border="1" data-bbox="605 422 1385 724"> <thead> <tr> <th>Mode</th> <th>Rank Select</th> <th>Bank Select 0</th> <th>Bank Select 1</th> <th>Bank Select 2</th> <th>Dimm Select</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>A19</td> <td>std</td> <td>A18</td> <td>A21</td> <td>A20</td> </tr> <tr> <td>001</td> <td>A20</td> <td>std</td> <td>A19</td> <td>A22</td> <td>A21</td> </tr> <tr> <td>010</td> <td>A18</td> <td>std</td> <td>A17</td> <td>A20</td> <td>A19</td> </tr> <tr> <td>011</td> <td>A17</td> <td>Std</td> <td>A16</td> <td>A19</td> <td>A18</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> <td>Reserved</td> <td>Reserved</td> <td></td> </tr> </tbody> </table> <p>Recommended Priority: 0, 1, 2</p> <p><b>Dual Channel Interleaved</b></p> <table border="1" data-bbox="605 804 1385 1106"> <thead> <tr> <th>Mode</th> <th>Rank Select</th> <th>Bank Select 0</th> <th>Bank Select 1</th> <th>Bank Select 2</th> <th>Dimm Select</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>A20</td> <td>std</td> <td>A19</td> <td>A22</td> <td>A21</td> </tr> <tr> <td>001</td> <td>A21</td> <td>Std</td> <td>A20</td> <td>A23</td> <td>A22</td> </tr> <tr> <td>010</td> <td>A19</td> <td>std</td> <td>A18</td> <td>A21</td> <td>A20</td> </tr> <tr> <td>011</td> <td>A18</td> <td>std</td> <td>A17</td> <td>A20</td> <td>A19</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> <td>Reserved</td> <td>Reserved</td> <td></td> </tr> </tbody> </table> <p>Recommended Priority: 2, 3, 0</p>	Mode	Rank Select	Bank Select 0	Bank Select 1	Bank Select 2	Dimm Select	000	A19	std	A18	A21	A20	001	A20	std	A19	A22	A21	010	A18	std	A17	A20	A19	011	A17	Std	A16	A19	A18	Others	Reserved	Reserved	Reserved	Reserved		Mode	Rank Select	Bank Select 0	Bank Select 1	Bank Select 2	Dimm Select	000	A20	std	A19	A22	A21	001	A21	Std	A20	A23	A22	010	A19	std	A18	A21	A20	011	A18	std	A17	A20	A19	Others	Reserved	Reserved	Reserved	Reserved	
		Mode	Rank Select	Bank Select 0	Bank Select 1	Bank Select 2	Dimm Select																																																																			
		000	A19	std	A18	A21	A20																																																																			
		001	A20	std	A19	A22	A21																																																																			
		010	A18	std	A17	A20	A19																																																																			
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		Others	Reserved	Reserved	Reserved	Reserved																																																																				
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010	A19	std	A18	A21	A20																																																																					
011	A18	std	A17	A20	A19																																																																					
Others	Reserved	Reserved	Reserved	Reserved																																																																						

### 3. Section 5.2.31 DCC – DRAM Channel Control

The following register bits definition replaces the *Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet*; Section 5.2.31

#### Section 5.2.31 DCC—DRAM Channel Control

MMIO Range: MCHBAR  
 Address Offset: 200h  
 Default Value: 00000000h  
 Access: RO, R/W  
 Size: 32 bits

This register controls how the DRAM channels work together. It affects how the CxDRB registers are interpreted and allows them to steer transactions to the correct channel.

Bit	Access and Default	Description
10	R/W 0 b	<b>Channel XOR Randomization Disable (CXRDIS):</b> When enabled, the DRAM Controller will try to spread page accesses evenly among the channels by including more address bits in the choice for which channel holds the requested address.  0: Channel XOR Randomization is enabled. CXRSEL's bit will be XORed with CHSEL's bit to pick the channel for a given address.  1: Channel XOR Randomization is disabled
9	R/W 0 b	<b>Channel XOR Randomization Control Bit (CXRSEL):</b> When Channel XOR Randomization is in use (see CXRDIS), the channel select will be randomized by XORing it with either host address bit 11 or 17.  0: Bit 11 will be XORed with the Channel Select bit  1: Bit 17 will be XORed with the Channel Select bit





#### 4. Section 7.2.33 GCFGC – Graphics Clock Frequency and Gating Control

The following register bits definition replaces the *Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet*; Section 7.2.33

#### Section 7.2.33 GCFGC—Graphics Clock Frequency and Gating Control

PCI Device: 2  
 Function: 0  
 Address Offset: F0h  
 Default Value: 0000h  
 Access: RO, R/W  
 Size: 16 bits

Bit	Access and Default	Description
15	R/W 0 b	<b>Graphics Display Clock Low Frequency Override</b> (For 915GMS only) 0 = Do not use Graphics cdclk low frequency override. 1 = Use Graphics cdclk = 152 MHz low frequency <b>Note:</b> This bit is reserved for 915GM and 910GML.
14	R/W 0 b	<b>Reserved</b>
13	R/W 0 b	GFX GVL low frequency Enable. 0 = Do not Use GFX GVL low frequency target for Render Clock. 1 = Use GFX GVL low frequency target for Render Clock.
12	R/W 0 b	GFX GVL low frequency target. 0 = 133 MHz (Default Value). 1 = Reserved.
11	R/W 0 b	Gate Core Render Clock (GCRC): 0: Core render clock (crclk) is running 1: Core render clock (crclk) is gated
10	R/W 0 b	Asynchronously Change Core Render Clock (ACCRC): A 0 to 1 transition on this bit will immediately load new pre- and post-divider values for the crclk and crx2clk. Writing 1 to 1, 1 to 0, and 0 to 0 have no effect.
9	R/W 0 b	Gate Core Display Clock (GCRC): 0: Core display clock (cdclk) is running 1: Core display clock (cdclk) is gated
8	R/W 0 b	Asynchronously Change Core Display Clock (ACDC): A 0 to 1 transition on this bit will immediately load new pre- and post-divider values for the cdclk. Writing 1 to 1, 1 to 0, and 0 to 0 have no effect.

Bit	Access and Default	Description
7	R/W 0 b	<b>Core Display Low Frequency Enable</b> 0 = Do not Use low frequency target for Display Clock. 1 = Use low frequency target (152 MHz) for Display Clock. (For 915GMS only) <b>NOTE: This bit is reserved for 915GM and 910GML.</b>
6:4	R/W 000 b	<b>Graphics Core Display Clock Select.</b> 000 = 190/200 MHz (Intel 915GM / 915GMS and Intel 910GML) 001 = 213/222 MHz (Intel 915GM only) 010 = Reserved 011 = Reserved 100 = 333 MHz (Intel 915GM @ 1.5 V only) 101 = Reserved 110 = Reserved 111 = Reserved
3	RO 0 b	<b>Reserved</b>
2:0	R/W 000 b	<b>Graphics Core Render Clock Select.</b> 000 = 160/166 MHz (Intel 915GM / 915GMS and Intel 910GML) 001 = 190/200 MHz (Intel 915GM) 010 = Reserved 011 = Reserved 100 = 333 MHz (Intel 915GM @ 1.5 V only) 101 = Reserved Others = Reserved.



5. **Section 5.1.23 C0DRT1 – Channel 0 DRAM Timing Register 1**

The following register bits definition replaces the *Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet*; Section 5.1.12

**Section 5.1.12 C0DRT1—Channel 0 DRAM Timing Register 1**

PCI Device: MCHBAR  
 Address Offset: 114h  
 Default Value: 00006111h  
 Access: RO, R/W  
 Size: 32 bits

Bit	Access and Default	Description
31:30	RO 00 b	<b>Reserved</b>
29:28	R/W 00 b	<p><b>Read to Pre-charge (tRTPC).</b>            These bits control the number of clocks that are inserted between a read command to a row pre-charge command to the same rank.</p> <p><b>Encoding tRP</b></p> <p>00: BL/2            01: Reserved            10: <b>Reserved</b>            11: <b>Reserved</b></p>
27:24	R/W 0 h	<b>Reserved</b>

Bit	Access and Default	Description
23:20	R/W 6 h	<p><b>Activate to Precharge delay (tRAS).</b></p> <p>This bit controls the number of DRAM clocks for tRAS. Minimum recommendations are beside their corresponding encodings.</p> <p>0000: Reserved            0001: Reserved            0010: Reserved            0011: Reserved            0100: 4 clocks            0101: 5 clocks            0110: 6 clocks            0111: 7 clocks (DDR333)            1000: 8 clocks            1001: 9 clocks (DDR 2 400)            1010: 10 clocks            1011: 11 clocks            1100: 12 clocks (DDR 2 533)            1101: 13 clocks            1110: 14 clocks            1111: 15 clocks</p> <p><b>Recommended values:</b></p> <p>7h DDR 333            9h DDR 2 400            Ch DDR 2 533</p>
19	RO 0 b	<b>Reserved</b>
18	R/W 0 b	<b>Reserved</b>
17	R/W 0 b	<p><b>Activate to Activate delay:</b></p> <p>Control Act to Act delay between the different banks of the same rank. Trr is specified in "ns". 10ns for 2KB page size and 7.5 ns for 1KB page</p> <p>0 = 2 Clock            1 = 3 Clock</p>



Bit	Access and Default	Description																		
16	R/W 0 b	<p><b>Pre-All to Activate Delay (tRPALL).</b></p> <p>This is applicable only to 8 bank architectures.</p> <p>Must be set to 1 if any Rank is populated with 8 bank device technology.</p> <p>0: tRPALL = tRP 1: tRPALL = tRP + 1</p>																		
15:11	R/W 01100 b	<p><b>Refresh Cycle Time (tRFC).</b></p> <p>Refresh cycle time is measured from a Refresh command (REF) until the first Activate command (ACT) to the same rank, required to perform a read or write.</p> <p style="text-align: center;"><b>DDR 2 tRFC spec</b></p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>tRFC</th> <th>256 Mb</th> <th>512 Mb</th> <th>1 Gb</th> </tr> </thead> <tbody> <tr> <td><b>DDR2 400 (5ns)</b></td> <td>75 ns = 15 clks</td> <td>105 ns = 21 clks</td> <td>127.5 ns = 26 clks</td> </tr> <tr> <td><b>DDR2 533 (3.75ns)</b></td> <td>75 ns = 20 clks</td> <td>105 ns = 28 clks</td> <td>127.5 ns = 34clks</td> </tr> </tbody> </table> <p style="text-align: center;"><b>DDR 1 tRFC spec</b></p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>tRFC</th> <th>64 Mb -512 Mb</th> <th>1 Gb</th> </tr> </thead> <tbody> <tr> <td><b>DDR 333 (6ns)</b></td> <td>75 ns = 13 clks</td> <td>120 ns = 20 clks</td> </tr> </tbody> </table> <p>00000b – 11111b Zero Clocks to Thirty-one Clocks respectively</p> <p>Actual clocks period depends on DDR clock frequency.</p> <p><b>Bios should round up. If the required clock count exceeds as allowed by this register, the bios should set this register to the max value and set corresponding bits in SDBUP.</b></p>	tRFC	256 Mb	512 Mb	1 Gb	<b>DDR2 400 (5ns)</b>	75 ns = 15 clks	105 ns = 21 clks	127.5 ns = 26 clks	<b>DDR2 533 (3.75ns)</b>	75 ns = 20 clks	105 ns = 28 clks	127.5 ns = 34clks	tRFC	64 Mb -512 Mb	1 Gb	<b>DDR 333 (6ns)</b>	75 ns = 13 clks	120 ns = 20 clks
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10	RO	<b>Reserved</b>																		
9:8	R/W 01 b	<p><b>CASB Latency (tCL).</b></p> <p>This value is programmable on DDR 2 SO-DIMM's. The value programmed here must match the CAS Latency of every DDR 2 SO-DIMM in the system.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Encoding</th> <th>DDR CL</th> <th>DDR2 CL</th> </tr> </thead> <tbody> <tr> <td>00:</td> <td>3</td> <td>5</td> </tr> <tr> <td>01:</td> <td>2.5</td> <td>4 (DDR2 533)</td> </tr> <tr> <td>10:</td> <td>Reserved</td> <td>3 (DDR2 400)</td> </tr> <tr> <td>11:</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table> <p><b>Note: Only the above recommended DDR2 timing values have been validated.</b></p>	Encoding	DDR CL	DDR2 CL	00:	3	5	01:	2.5	4 (DDR2 533)	10:	Reserved	3 (DDR2 400)	11:	Reserved	Reserved			
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11:	Reserved	Reserved																		
7	RO	<b>Reserved</b>																		

Bit	Access and Default	Description																		
6:4	R/W 001 b	<p><b>DRAM RASB to CASB Delay (tRCD).</b></p> <p>This bit controls the number of clocks inserted between a row activate command and a read or write command to that row.</p> <table border="0"> <tr> <td>Encoding</td> <td>DDR tRCD</td> <td>DDR2 tRCD</td> </tr> <tr> <td>000:</td> <td>2</td> <td>2 clocks</td> </tr> <tr> <td>001:</td> <td>3</td> <td>3 clocks (DDR2 400)</td> </tr> <tr> <td>010:</td> <td>4</td> <td>4 clocks (DDR2 533)</td> </tr> <tr> <td>011:</td> <td>5</td> <td>5 clocks</td> </tr> <tr> <td>100 - 111:</td> <td>Reserved</td> <td>Reserved</td> </tr> </table> <p><b>Note:</b> Only the above recommended DDR2 timing values have been validated.</p>	Encoding	DDR tRCD	DDR2 tRCD	000:	2	2 clocks	001:	3	3 clocks (DDR2 400)	010:	4	4 clocks (DDR2 533)	011:	5	5 clocks	100 - 111:	Reserved	Reserved
Encoding	DDR tRCD	DDR2 tRCD																		
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010:	4	4 clocks (DDR2 533)																		
011:	5	5 clocks																		
100 - 111:	Reserved	Reserved																		
3	RO	<b>Reserved</b>																		
2:0	R/W 001 b	<p><b>DRAM RASB Precharge (tRP).</b></p> <p>This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same rank.</p> <table border="0"> <tr> <td>Encoding</td> <td>DDR tRP</td> <td>DDR2 tRP</td> </tr> <tr> <td>000:</td> <td>2</td> <td>2 Clocks</td> </tr> <tr> <td>001:</td> <td>3</td> <td>3 Clocks (DDR2 400)</td> </tr> <tr> <td>010:</td> <td>4</td> <td>4 Clocks (DDR2 533)</td> </tr> <tr> <td>011:</td> <td>5</td> <td>5 Clocks</td> </tr> <tr> <td>100 - 111:</td> <td>Reserved</td> <td></td> </tr> </table> <p><b>Note:</b> Only the above recommended DDR2 timing values have been validated.</p>	Encoding	DDR tRP	DDR2 tRP	000:	2	2 Clocks	001:	3	3 Clocks (DDR2 400)	010:	4	4 Clocks (DDR2 533)	011:	5	5 Clocks	100 - 111:	Reserved	
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