NANO-5050

NANO-ITX Board

User's Manual

Version 1.0

Table of Contents

How to Use This Manual

How to Use This Manual

The manual describes how to configure your NANO-5050 system to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Board Computer.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single board computer.

Chapter 2 : Hardware Configuration. Shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3 : System Installation. Describes how to properly mount the CPU, main memory and Compact Flash to get a safe installation and provides a programming guide of Watch Dog Timer function.

Chapter 4 : BIOS Setup Information. Specifies the meaning of each setup parameters, how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give users some guidelines of trouble-shooting.

Chapter 5 : Troubleshooting. Provides various useful tips to quickly get NANO-5050 running with success. As basic hardware installation has been addressed in Chapter 3, this chapter will basically focus on system integration issues, in terms of backplane setup, BIOS setting, and OS diagnostics.

The content of this manual and EC declaration document is subject to change without prior notice. These changes will be incorporated in new editions of the document. **Portwell** may make supplement or change in the products described in this document at any time.

Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site :
http://www.portwell.com.tw/.

Chapter 1
System Overview

1.1 Introduction

Portwell Inc., a world-leading innovator in the Industrial PC (IPC) market and a member of the Intel® Communications Alliance, has launched its new NANO-ITX form factor based NANO-5050 for embedded system board (ESB) that offers a smaller footprint, lower power consumption, robust computing power and with longevity support.

The NANO-5050 is specifically designed to operate at very low power consumption and low heat, so it can be a truly fanless configuration and battery operated. Base on Intel® System Controller Hub NM10, the NANO-5050 supports one DDR3 SODIMM socket up to 4GB system memory and comes with one SATA II, one Mini-PCIe socket, triple independent display by VGA, DP and 18/24-bit LVDS (dual display at the same time), one gigabit Ethernet, one CF-SATA socket and Six USB 2.0 ports (two ports are on rear IO). It also built with DC 12V or ATX 12V input.

Base on leading Intel® Atom solution, NANO-5050 is a compact and low power dissipation board for Digital Signage, Digital Security Surveillance (DSS) and Medical applications…etc.

1.2 Check List

The NANO-5050 package should cover the following basic items

- ✓ One NANO-5050 NANO-ITX Main Board
- ✓ One passive Heatsink
- ✓ One Installation Resources CD-Title
- ✓ One SATA cable

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintain

1.3 Product Specification

- **Main Processor**
  - On board Intel® ATOM™ D2550 1.86GHz processor
- **Chipset**
  - Intel® System Controller Hub NM10

- **System BIOS**
  - Phoenix uEFI BIOS
- **Main Memory**
  - One 204pin DDR3 SODIMM socket on board up to 4GB system memory
- **Power input**
  - DC 12V input on rear I/O
  - 4pin +12V power connector on board
  - (DC 12V Jack and 4pin power connector can't be used at the same time)
- **Serial Port**
  - Support one RS232/422/485 port on-board connector (adjust by bios)
- **USB Interface**
  - Support six USB 2.0 (Universal Serial Bus) ports, two on rear I/O and four on board header for internal devices.
- **SATA Interface**
  - Support one SATA II ports
- **CF-SATA interface**
  - Support one CF-SATA socket
  - Support both CF card and CF-SATA card
- **Audio Interface**
  - Mic-In and Line-Out Audio Jack on rear I/O
- **Watch Dog Timer**
  - Support WDT function through software programming for enable/disable and interval setting
  - General system reset
- **Display**
  - Support triple independent display by DP (rear I/O), VGA (on-board connector) and single channel 18/24-bit LVDS
  - Only support dual display simultaneously
- **On-board Ethernet LAN**
  - One Gigabit Ethernet (10/100/1000 Mbits/sec) LAN port using Intel 82583V PCI-Expressx1 interface GbE Controller
  - Support Wake on LAN function
- **High Drive GPIO**
  - On-board programmable 8-bit Digital I/O interface
- **Cooling Fans**
  - Support one 3-pin power connector for system fan
- **System Monitoring Feature**
  - Monitor system temperature and major power sources.
- **Outline Dimension (L x W)**
  - 120mm(4.72'') x 120mm(4.72'')

1.4 System Configuration

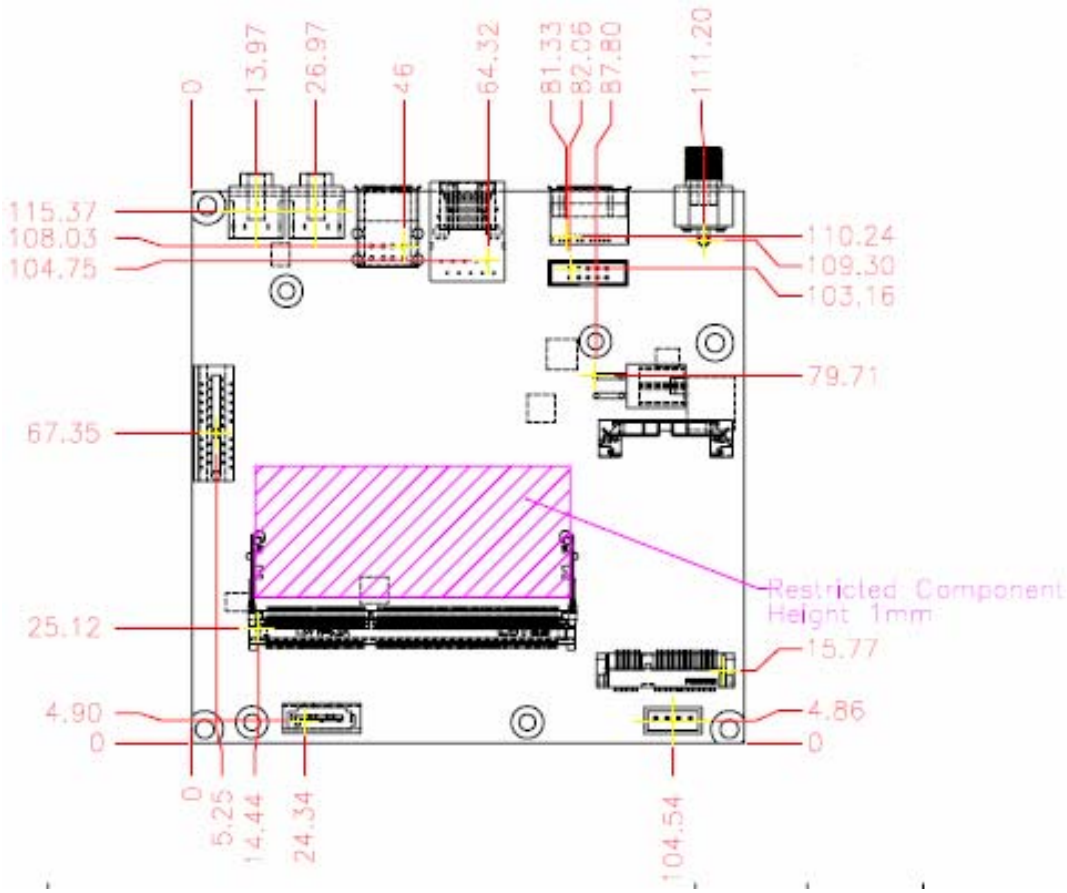
System Configuration	
CPU Type	Intel® Atom™ CPU D2550 @1.86GHz L2:1024K
SBC BIOS	Portwell, Inc. NANO-5050 Rev.:R1.00.W2(12112012)
Memory	Transcend DDR3 1066 SODIMM 4G*1 (hynix H5TQ2G83AFR)
VGA Card	Onboard Intel® Graphics Media Accelerator 3600 Series
VGA Driver	Intel® Graphics Media Accelerator 3600 Series Ver:8.14.8.1075
LAN Card	Onboard Intel® 82583V Gigabit Network Connection
LAN Driver	Intel® 82583V Gigabit Network Connection Ver:11.17.27.0
Audio Card	Onboard Realtek ALC886 High Definition Audio
Audio Driver	Realtek ALC886 High Definition Audio Ver:6.0.1.6526
Chip Driver	Intel® Chipset Device Software Ver:9.2.2.1029
SATA HDD	Seagate ST3160316AS 160GB
Compact Flash	Apacer AP-CF001GP4CG-NR
USB CDROM	ASUS CB-5216A-U
Power Supply	FSP150-50PL1

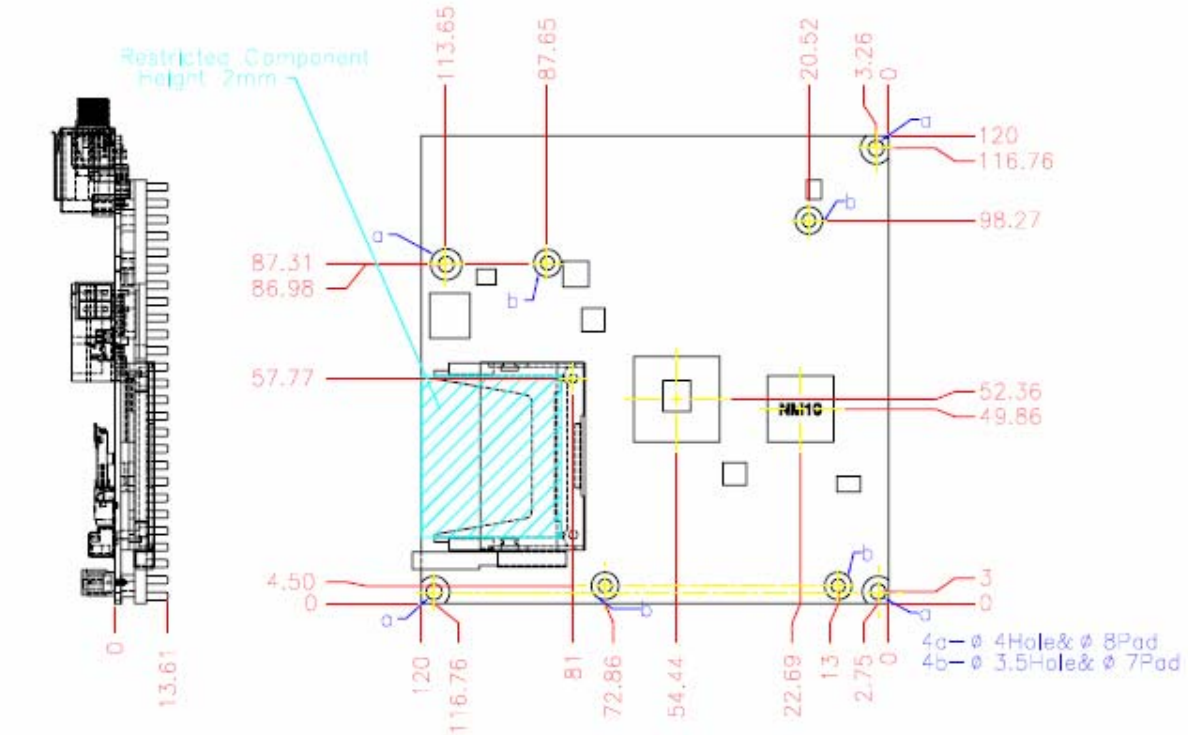
- **Power Consumption test:** Run Burning Test V6.0
  RUN time: 10 / 30 Minutes.

Item	Power ON	Full Loading 10Min	Full Loading 30Min
DC +12V	**1.41**	**1.84**	**1.86**

- **Operating Temperature**
  0°C ~ 55°C
- **Storage temperature**
  -20 ~ 85 °C
- **Relative Humidity**
  0% ~ 95%, non-condensing

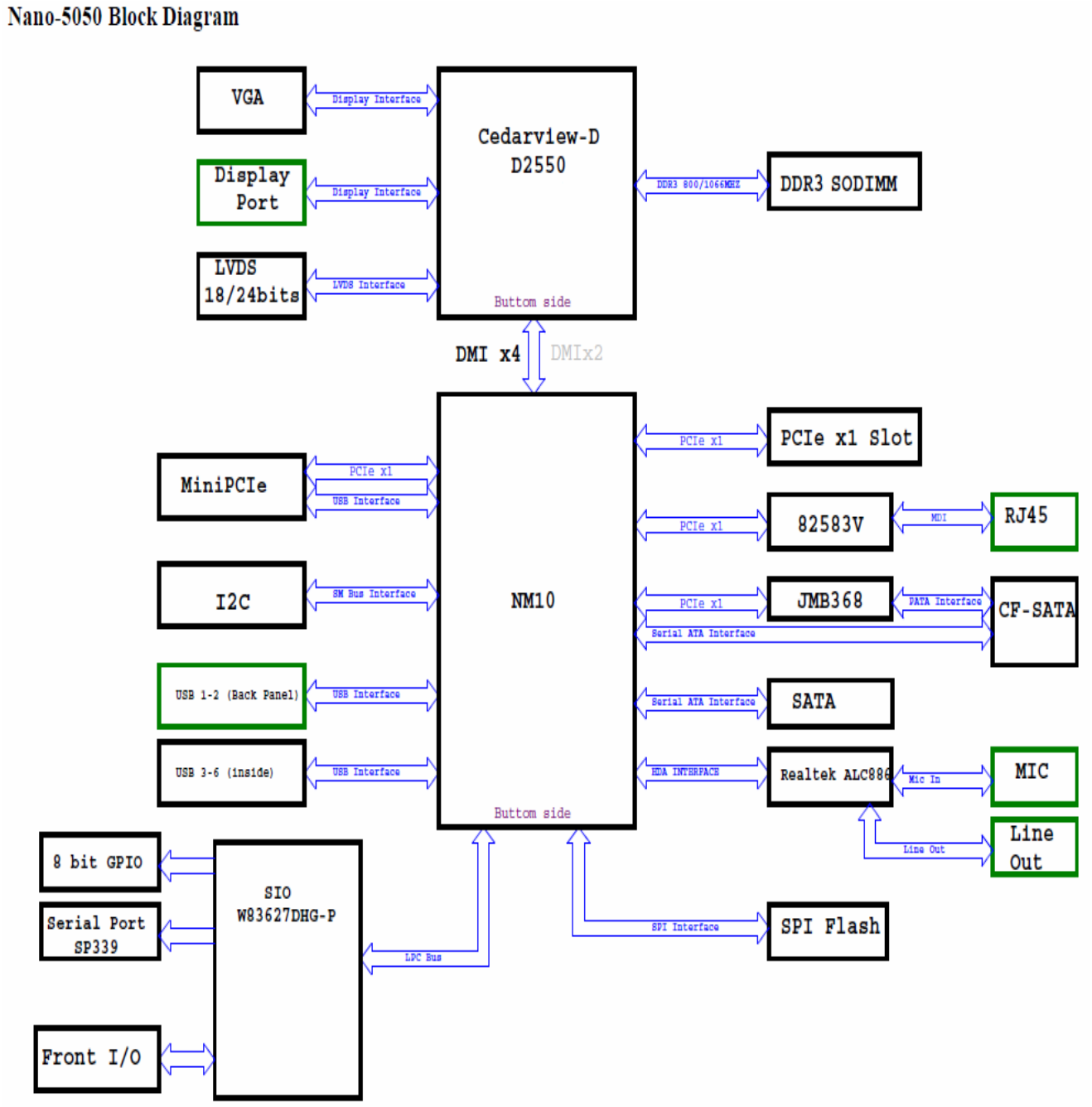
1.4.1 Mechanical Drawing





1.5 System Architecture

All of details operating relations are shown in NANO-5050 System Block Diagram.



NANO-5050 System Block Diagram

Chapter 2
Hardware Configuration

This chapter gives the definitions and shows the positions of jumpers, headers and connector. All of the configuration jumpers on NANO-5050 are in the proper position. The default settings are indicated with a star sign (★).

2.1 Jumper Setting

In the following sections, **Short** means covering a jumper cap over jumper pins; **Open** or **N/C** (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 2-1 for the Jumper allocations.

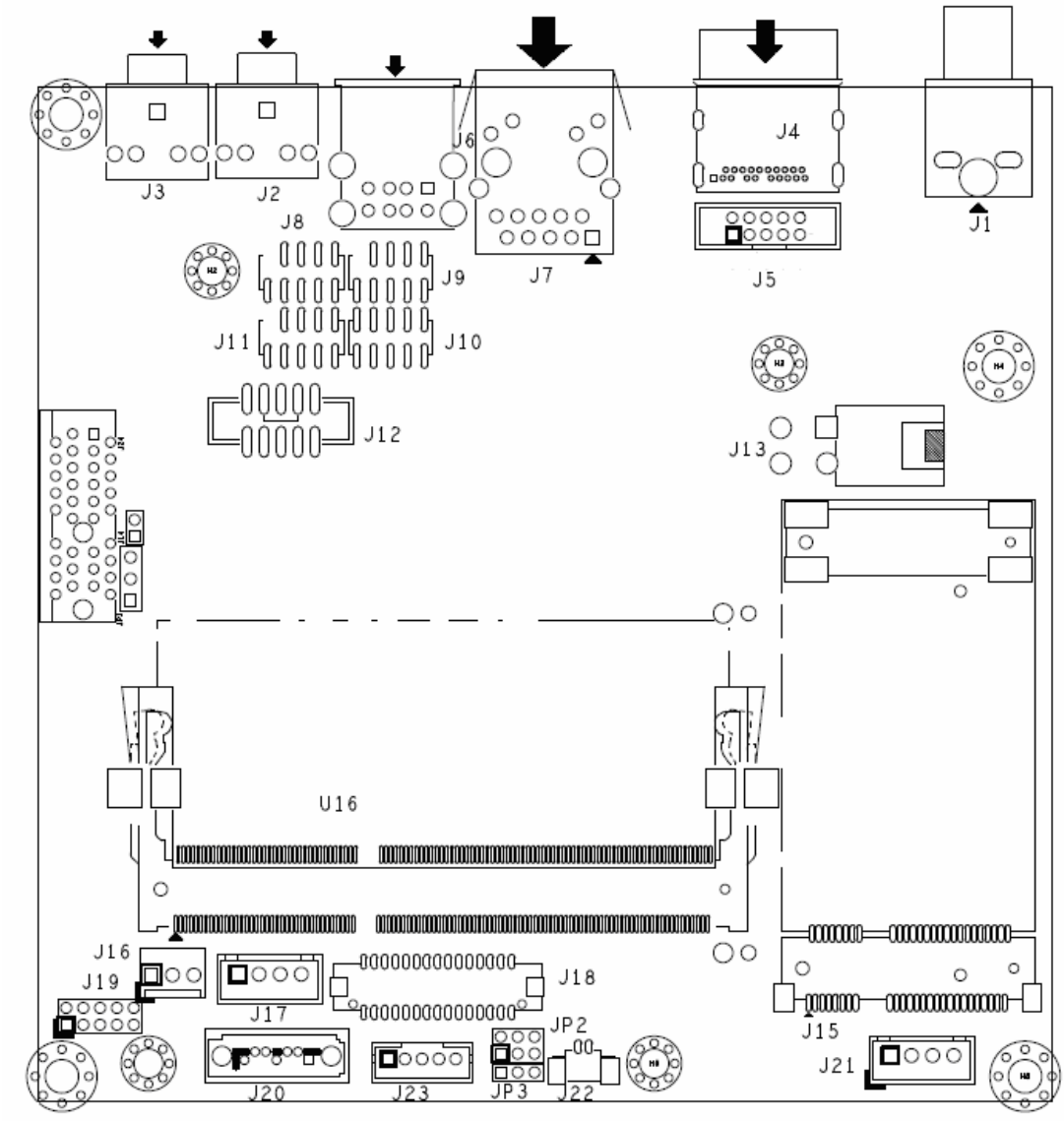


Figure 2-1 NANO-5050 Jumper and Connector Locations (Top)

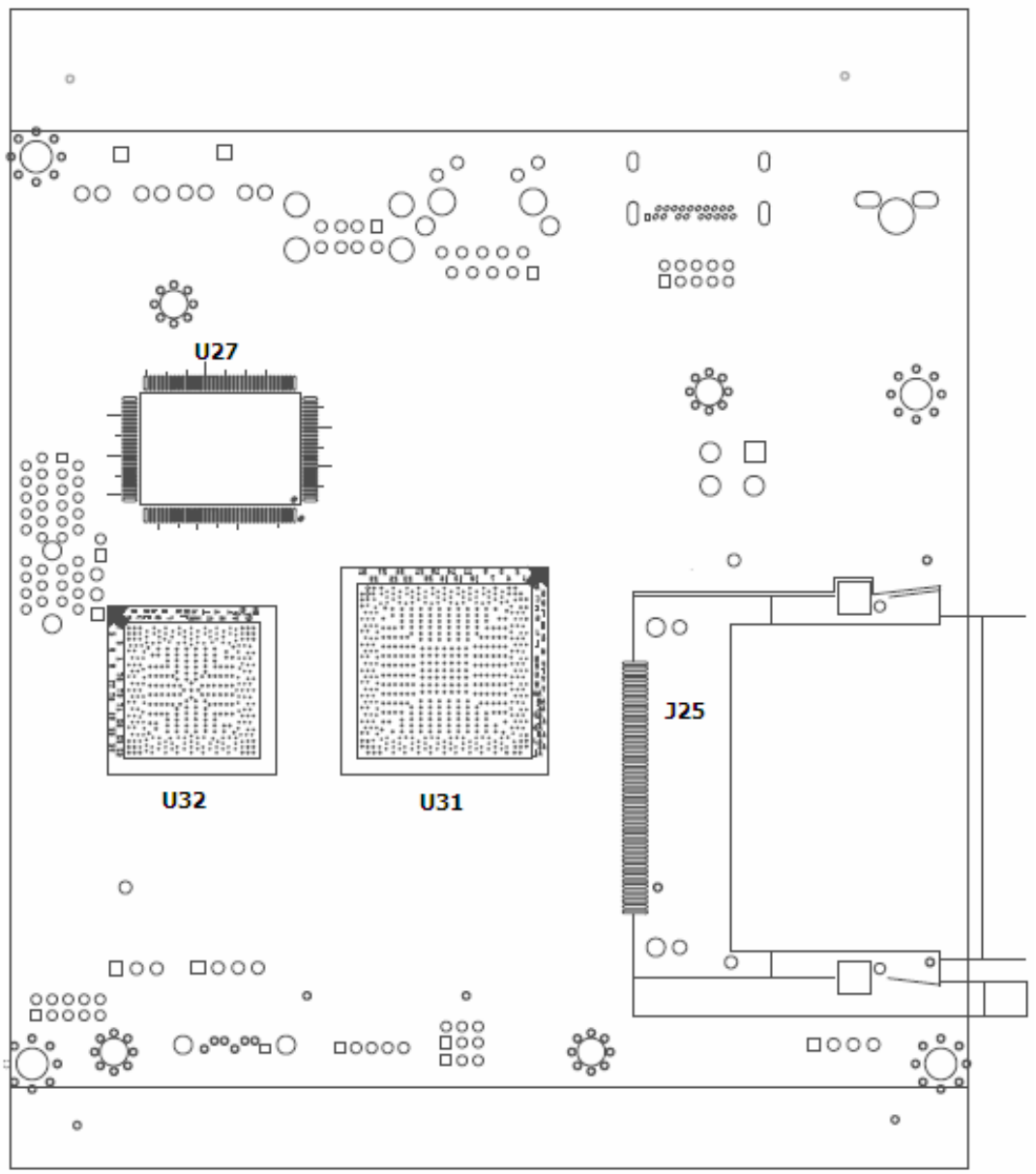


Figure 2-2 NANO-5050 Jumper and Connector Locations (Bottom)

2.2 Connectors

I/O peripheral devices are connected to the interface connectors.

Connector	Function	Remark
J1	+12V DC adapter	
J2	Line Out	
J3	Mic In	
J4	Display Port	
J5	CRT display	
J6	USB	
J7	LAN	

J8	reserve USB	
J9	reserve USB	
J10	8 bits GPIO	
J11	LPC debug port	
J12	Serial Port	
J13	+12V DC source	
J14	reserve	
J15	Mini PCIe	
J16	Rear side FAN	
J17	SATA power	
J18	LVDS pane	
J19	LED/Switch	
J20	SATA	
J21	SM Bus	
J22	Coin battery	
J23	Panel back light	
J24	PCIe x1	
J25	CF-SATA (button side)	
JP1	Clean RTC(Default 1-2)	
JP2	LVDS Power Level (Default 1-2)	
JP3	LVDS Back-light enable level high/low (Default 1-2)	

Pin Assignments of Connectors

J1 : reserve for +12V DC adapter

PIN No.	Signal Description
1	12V
2	GND
3	GND

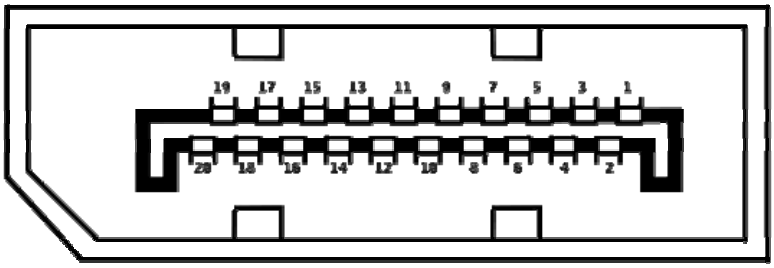
J2 : Line Out

PIN No.	Signal Description
1	GND
2	Line Out L
3	GND
4	Jack Detect
5	Line Out R

J3 : Mic In

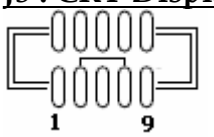
PIN No.	Signal Description
1	GND
2	Mic In L
3	GND
4	Jack Detect
5	Mic In R

J4 : Display Port



PIN No.	Signal Description	PIN No.	Signal Description
1	Lane0+	2	GND
3	Lane0-	4	Lane1+
5	GND	6	Lane1-
7	Lane2+	8	GND
9	Lane2-	10	Lane3+
11	GND	12	Lane3-
13	CONFIG1	14	CONFIG2
15	AUX_CH+	16	GND
17	AUX_CH-	18	Hot Plug
19	Return for Power	20	DP Power 3.3V/500mA

J5 : CRT Display



PIN No.	Signal Description	PIN No.	Signal Description
1	RED	2	DDCCLK
3	GREEN	4	A_Ground
5	BLUE	6	DDCDATA
7	VSYNC	8	D_Ground
9	HSYNC	10	DDC_VCC

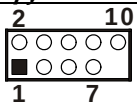
J6 : USB

PIN No.	Signal Description	PIN No.	Signal Description
A1	+5V	B1	+5V
A2	USBD0-1N	B2	USBD0-1N
A3	USBD0-1P	B3	USBD0-1P
A4	Ground	B4	Ground

J7 : LAN(RJ45)

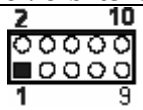
PIN No.	Signal Description
1	L1_MDIP0
2	L1_MDIN0
3	L1_MDIP1
4	L1_MDIP2
5	L1_MDIN2
6	L1_MDIN1
7	L1_MDIP3
8	L1_MDIN3

J8/JP : reserve USB



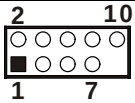
PIN No.	Signal Description	PIN No.	Signal Description
1	+5V	2	+5V
3	USBD-	4	USBD-
5	USBD+	6	USBD+
7	GND	8	GND
		10	NC

J10 : 8 bits GPIO



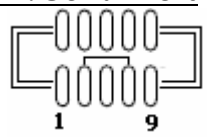
PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO0	2	GPIO4
3	GPIO1	4	GPIO5
5	GPIO2	6	GPIO6
7	GPIO3	8	GPIO7
9	GND	10	VCC

J11 : LPC debug Po



PIN No.	Signal Description	PIN No.	Signal Description
1	LAD0	2	+3.3V
3	LAD1	4	RST#
5	LAD2	6	LFRAME#
7	LAD3	8	33MHzCLK
		10	GND

J12 : Serial Port



RS-232 Mode:

PIN No.	Signal Description	PIN No.	Signal Description
1	Data Carrier Detect (DCD)	2	Receive Data (RXD)
3	Transmit Data (TXD)	4	Data Terminal Ready (DTR)
5	GND	6	Data Set Ready (DSR
7	Request to Send (RTS)	8	Clear to Send (CTS)
9	Ring Indicator (RI		

RS-422/485 Mode:

PIN No.	Signal Description	PIN No.	Signal Description
1	TxD-/RxD-	2	TxD+/RxD
3	RxD+(422 only)	4	RxD-(422 only)
5	GND		

J13 : +12V DC Source

PIN No.	Signal Description
1	GND
2	GND
3	+12V
4	+12V

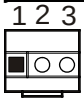
J14 : Reserve

J15 : Mini PCIe

PIN No.	Signal Description	PIN No.	Signal Description
1	Wake#	2	3.3V
3	Reserved	4	GND
5	Reserved	6	1.5V

7	CLKREQ#	8	Reserved
9	GND	10	Reserved
11	REFCLK-	12	Reserved
13	REFCLK+	14	Reserved
15	GND	16	Reserved
KEY			
17	Reserved	18	GND
19	Reserved	20	Reserved
21	GND	22	PERST#
23	PE_R_0-	24	+3.3Vaux
25	PE_R_0+	26	GND
27	GND	28	1.5V
29	GND	30	SMB_CLK
31	PE_T_0-	32	SMB_DAT
33	PE_T_0+	34	GND
35	GND	36	USB_D-
37	Reserved	38	USB_D+
39	Reserved	40	GND
41	Reserved	42	LED_WAN#
43	Reserved	44	LED_LAN#
45	Reserved	46	LED_PAN#
47	Reserved	48	1.5V
49	Reserved	50	GND
51	Reserved	52	3.3V

J16 : Rear Side FAN



PIN No.	Signal Description
1	Ground
2	+12V
3	Fan Speed Detecting signal

J17 : SATA Power

PIN No.	Signal Description
1	+12V
2	GND
3	GND
4	+5V

J18 : LVDS Panel

PIN No.	Signal Description	PIN No.	Signal Description
1	LVDS_DATA0	2	LVDS_DATA#0
3	LVDS_DATA1	4	LVDS_DATA#1
5	LVDS_DATA2	6	LVDS_DATA#2
7	LVDS_DATA3	8	LVDS_DATA#3
9	LVDS_CLK	10	LVDS_CLK#
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	NC	18	NC
19	NC	20	NC
21	LVDS_DDC_CLK	22	LVDS_DDC_DATA
23	GND	24	NC
25	GND	26	GND
27	VDD_LVDS	28	VDD_LVDS
29	NC	30	VDD_LVDS

J19 : LED/Switch

PIN No.	Signal Description	PIN No.	Signal Description
1	WR_LED-	2	LVDS_DATA#0
3	SUS_LED+	4	LVDS_DATA#1
5	HDD_LED+	6	HDD_LED
7	RST_BTN	8	GND
9	GND	10	PWR_BTN

J20 : SATA

PIN No.	Signal Description
1	GND
2	DF_SATA_TX+0
3	DF_SATA_TX-0
4	GND
5	DF_SATA_RX-0
6	DF_SATA_RX+0
7	GND

J21 : SM BUS

PIN No.	Signal Description
1	SM_CLK
2	SM_DATA
3	GND
4	3.3V

J22 : Coin Battery

PIN No.	Signal Description
1	Positive
2	Negative

J23 : Panel back light

PIN No.	Signal Description
1	+5V
2	GND/PWM
3	+12V
4	GND
5	BACKLIGH_EN/EN#

J24 : PCIe x 1

PIN No.	Signal Description	PIN No.	Signal Description
A1	SMBCLK	B1	+12V
A2	+12V	B2	+12V
A3	+12V	B3	+12V
A4	GND	B4	GND
A5	DF_PCIE_TXP2	B5	DF_ PCIE_CLKP
A6	DF_PCIE_TXN2	B6	DF_ PCIE_CLKN2
A7	DF_PCIE_RXP2	B7	GND
A8	DF_PCIE_RXN2	B8	+3.3V
A9	+3.3V	B9	CLKREQ2#
A10	+3.3V	B10	+3.3V_AUX
A11	RST#	B11	PCIE_WAKE#
A12	GND	B12	SMBDATA
A13	DF_ PCIE_CLKP1	B13	GND
A14	DF_ PCIE_CLKN1	B14	DF_PCIE_TXP1
A15	GND	B15	DF_PCIE_TXN1
A16	DF_PCIE_RXP1	B16	GND
A17	DF_PCIE_RXN1	B17	CLKREQ1#
A18	GND	B18	GND

J25 : CF-SATA

PIN No.	Signal Description	PIN No.	Signal Description
1	GND	26	CD1#
2	D3	27	D11
3	D4	28	D12
4	D5	29	D13
5	D6	30	D14
6	D7	31	D15
7	CS0#	32	CS1#
8	GND	33	VS1#
9	ATASEL#	34	IOR#

10	SATA_TX+	35	IOW#
11	SATA_TX-	36	WE#
12	GND	37	INTR
13	VCC	38	VCC
14	GND	39	CSEL#
15	SATA_RX-	40	VS2#
16	SATA_RX+	41	RESET#
17	GND	42	IORDY
18	A2	43	DMARQ
19	A1	44	DMACK#
20	A0	45	DASP#
21	D0	46	PDIAG#
22	D1	47	D8
23	D2	48	D9
24	IOCS16#	49	D10
25	CD2#	50	GND

JP1 : Clean RTC

PIN No.	Function
1-2	Positive
2-3	Negative

JP2 : Panel Power Level

PIN No.	Process Selection
1-2	3.3V ★
3-4	5V
5-6	12V

JP3 : Backlight enable signal type

PIN No.	Process Selection
1-2	High enable ★
2-3	Low enable

Chapter 3
System Installation

This chapter provides you with instructions to set up your system. The additional information is enclosed to help you set up onboard PCI device and handle Watch Dog Timer (WDT) and operation of GPIO in software programming.

3.1 Intel ® Atom ™ Processor D2550

Passively-cooled, soldered-down Dual-Core Intel ® Atom™ processor D2550 with integrated graphics and integrated memory controller that's suitable for fanless system and low-watt design.

3.2 Main Memory

NANO-5050 provide 1 x 204-pin SO-DIMM sockets which supports 800/1066 MHz DDR3-SDRAM as main memory, Non-ECC (Error Checking and Correcting), non-register functions. The maximum memory size can be up to 4GB capacity. Memory clock and related settings can be detected by BIOS via SPD interface.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedures to install memory module into memory socket. Before locking, make sure that all modules have been fully inserted into the card slots.

Note: DDR3 1333 MHz and DDR3 1600 MHz memory will run at 1066 MHz

3.3 Installing Single Board Computer

To install your NANO-5050 into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position
Step 2 : Install memory module onto memory socket
Step 3 : Place NANO-5050 into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

WARNING
Please ensure that SBC is properly inserted and fixed by mechanism.

Note:
Please refer to section 3.3.1 to 3.3.7 to install INF/VGA/LAN/Audio drivers.

3.3.1 Chipset Component Driver

The chipset on NANO-5050 is a new chipset that a few old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows 7, please install its INF driver before any other drivers installation. You can easily find the chipset component driver in NANO-5050 VGTAM CD-title.

3.3.2 Intell®Integrated Graphics

The Intel ® Atom TM Processor D2550 contains an integrated graphics core, the Intel ® GMA 3650 graphics controller. This combination makes NANO-5050 an excellent piece of multimedia hardware, NANO-5050 supports VGA, DP and also LVDS out put. The VGA port supports analog displays. The maximum supported resolution is 1920 x 1200 (WUXGA) at a 60 Hz refresh rate. VGA port enabled from POST whenever monitor is connected.

Drivers Support

Please find Intel® GMA 3650 driver in NANO-5050 CD-title. Driver supports Windows 7 only.

3.3.3 Intel Gigabit Ethernet Controller

Drivers Support

Please find Intel 82583V Ethernet driver in /Ethernet directory of NANO-5050 CD-title. The drivers support Windows 7.

LED Indicator

NANO-5050 provides two LED indicators to report Intel 82583MM Gigabit Ethernet interface status. Please refer to the table below as a quick reference guide.

82583V	Color	Name of LED	Operation of Ethernet Port		
			Linked	Active	
Status LED	Green	LAN Linked & Active LED	On	Blinking	
Speed LED	Orange & Green	LAN speed LED	Giga Mbps	100 Mbps	10 Mbps

3.3.4 Audio Controller

Please find Realtek ALC886-GR Audio driver form NANO-5050 CD-title. The drivers support Windows 7.

3.4 Clear CMOS Operation

The following table indicates how to enable/disable Clear CMOS Function hardware circuit by putting jumpers at proper position.

J14:CMOS Setup (1*3 Pin Header/2.0 mm)

PIN No	Description
1-2 Short	Normal Operation ★
2-3 Short	Clear CMOS contents

3.5 WDT Function

The Watchdog Timer of motherboard consists of 8-bit programmable time-out counter and a control and status register. Reference Winbond Super I/O W83627DHG-PT Spec chapter 16. The units of Watchdog Timer counter are selected at Logical Device 8, CR〔F5h〕, bit〔3〕. The time-out value is set ar Logical Device 8, CR〔F6h〕. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

WDT Control Command Example

```
#include <stdio.h>
#include <stdlib.h>
#include <conio.h>
#include <dos.h>

void change_LDN (unsigned char LDN)
{
   outportb(0x2E, 0x07);
   outportb(0x2F, LDN);
}
void set_CFG (unsigned char Add, unsigned char Value)
{
   outportb (0x2E, Add);
   outportb (0x2F, Value);
}

int main(void)
{
      unsigned char temp;
   // Initialze WDT function
      temp = get_CFG (0x2D) & ~0x01;
      set_CFG (0x2D, temp);

   change_LDN (0x08);
```

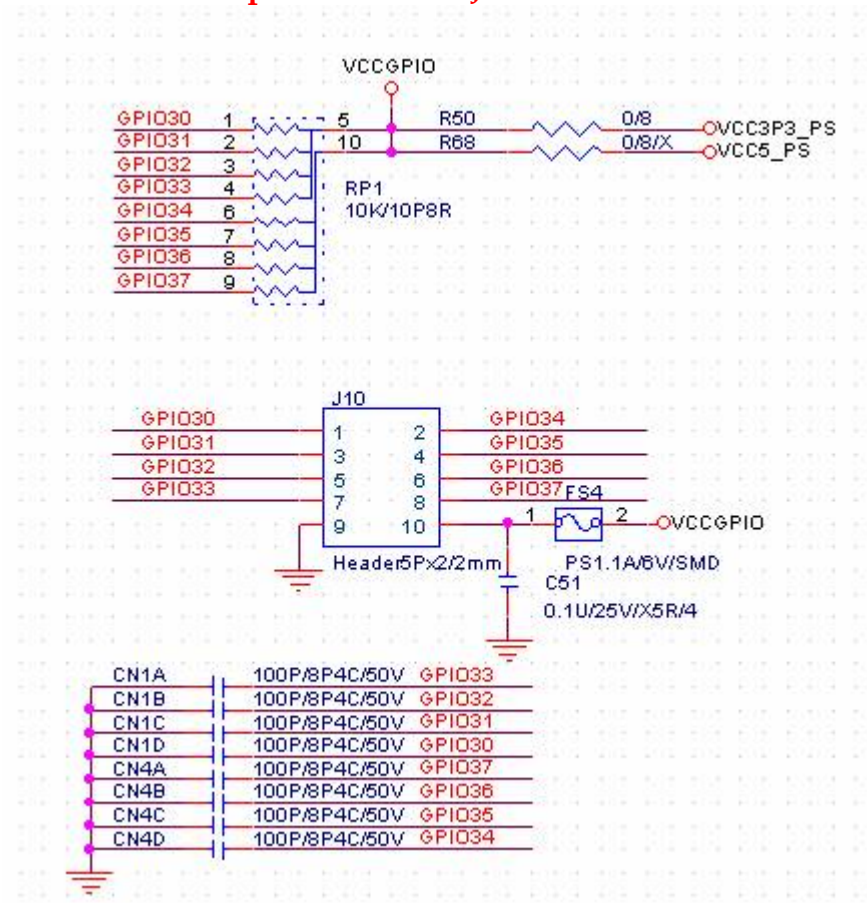
```
    set_CFG (0x30, 0x01);
    set_CFG (0xF5, 0x00);
    set_CFG (0xF7, 0x00);

    printf ("Trigger WDT with 5 sec...will reboot in 5 sec.\n");
    printf ("Press Enter to disable WDT...\n");
    set_CFG (0xF6, 0x05);
    getchar ();
    set_CFG (0xF6, 0x00);

    printf ("All test complete. Press Enter to EXIT.");

    getchar();
       return 0;
}
```

3.6 GPIO

The motherboard provides 8 input / output ports that can be individually configured to perform a simple basic I/O function.

GPIO Pin Assignment
The NANO-5050 provides 8 input/output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be made. Port values can be set to read or write through Data Register.
The GPIO port is located on J10 shown as follows.

WARNING
Do not short the pin 9 and 10 of J10!




```
#include <stdio.h>
#include <stdlib.h>
#include <conio.h>
#include <dos.h>

void enter_SIO()
{
```

```
    outportb(0x2E, 0x87);
    outportb(0x2E, 0x87);
}

void exit_SIO ()
{
    outportb(0x2E, 0xAA);
}


void change_LDN (unsigned char LDN)
{
    outportb (0x2E, 0x07);
    outportb (0x2F, LDN);
}

unsigned char get_CFG (unsigned char Add)
{
    outportb (0x2E, Add);
    return inportb (0x2F);
}

void set_CFG (unsigned char Add, unsigned char Value)
{
    outportb (0x2E, Add);
    outportb (0x2F, Value);
}

void main (void)
{
    unsigned char tmpData = 0x0;

    printf("==== NANO-5050 GPIO test program ====\n");

    enter_SIO();
       // Initialze GPIO function
       set_cfg (0x2C, get_cfg (0x2C) & ~0xE0; );

    // Switch to LDN9 for GPIO3
    change_LDN(0x09);
       // Enable GPIO3 function
    set_CFG (0x30, (get_CFG (0x30) | 0x02));
    set_CFG (0xF9, 0x00);
    set_CFG (0xFE, 0x70);


    // printf("Set GP1~4 to INPUT, GP5~8 to OUTPUT\n");
    set_CFG (0xF0, 0xF0);
    // printf("Set GP5~8 HIGH\n");
```

```
    set_CFG (0xF1, 0x0F);
    // printf("Read GP1~4:");
    tmpData = get_CFG(0xF1);

    // printf("data: 0x%X ", tmpData);
    if(tmpData == 0xFF)
       printf ("PASS!\n");
    else
       printf ("FAIL!\n");

    // printf("Set GP5~8 LOW\n");
    set_CFG(0xF1, 0x00);
    // printf("Read GP1~4:");
    tmpData = get_CFG(0xF1);
    // printf("data: 0x%X ", tmpData);
    if(tmpData == 0x00)
       printf("PASS!\n");
    else
       printf("FAIL!\n");

    // printf("Set GP1~4 to OUTPUT, GP5~8 to INPUT\n");
    set_CFG(0xF0, 0x0F);
    // printf("Set GP1~4 to HIGH\n");
    set_CFG(0xF1, 0xF0);
    // printf("Read GP5~8:");
    tmpData = get_CFG(0xF1);
    // printf("data: 0x%X ", tmpData);
    if(tmpData == 0xFF)
       printf("PASS!\n");
    else
       printf("FAIL!\n");

    // printf("Set GP1~4 LOW\n");
    set_CFG(0xF1, 0x00);
    // printf("Read GP5~8:");
    tmpData = get_CFG(0xF1);
    // printf("data: 0x%X ", tmpData);
    if(tmpData == 0x00)
       printf("PASS!\n");
    else
       printf("FAIL!\n");

getchar();

}
```

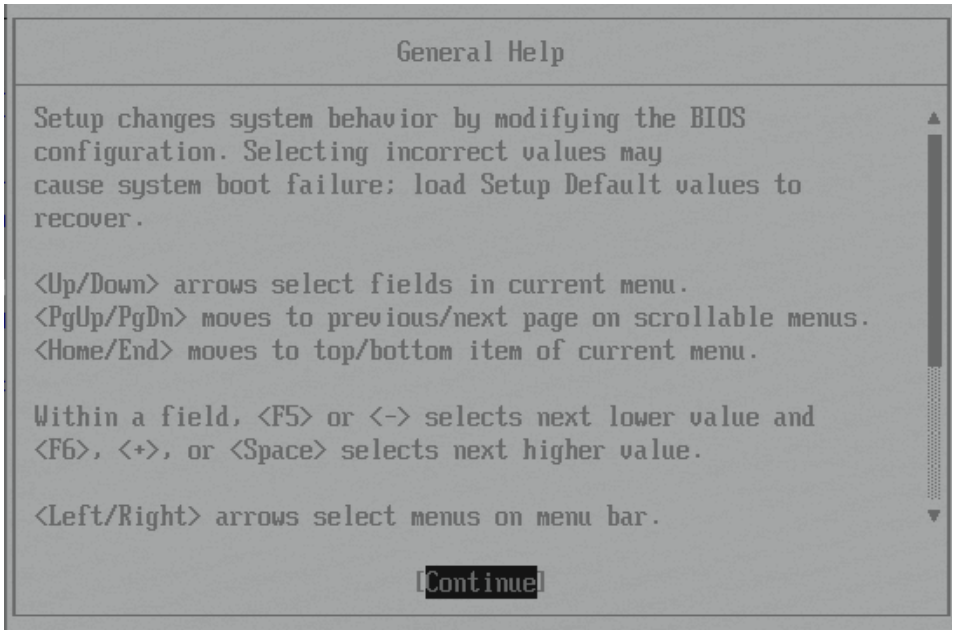
Chapter 4
BIOS Setup Information

NANO-5050 equipped with the Phoenix BIOS stored in SPI Flash. BIOS has built-in setup program that allows users to adjust the basic system configuration. This type of information is stored in CMOS RAM that it is retained even if power-off periods. When system turns on, NANO-5050 communicates with peripheral devices and checks its hardware resources referring to the configuration information stored in CMOS memory. If any error occurs, or CMOS parameters need to be defined, the diagnostic program will prompt to user to enter the SETUP program. Some errors are significant that'll abort the start-up process too.

4.1 Entering Setup

Turn on or reboot the computer. When the message "Hit <F2> if you want to run SETUP" appears, press <F2> key immediately to enter BIOS setup program.

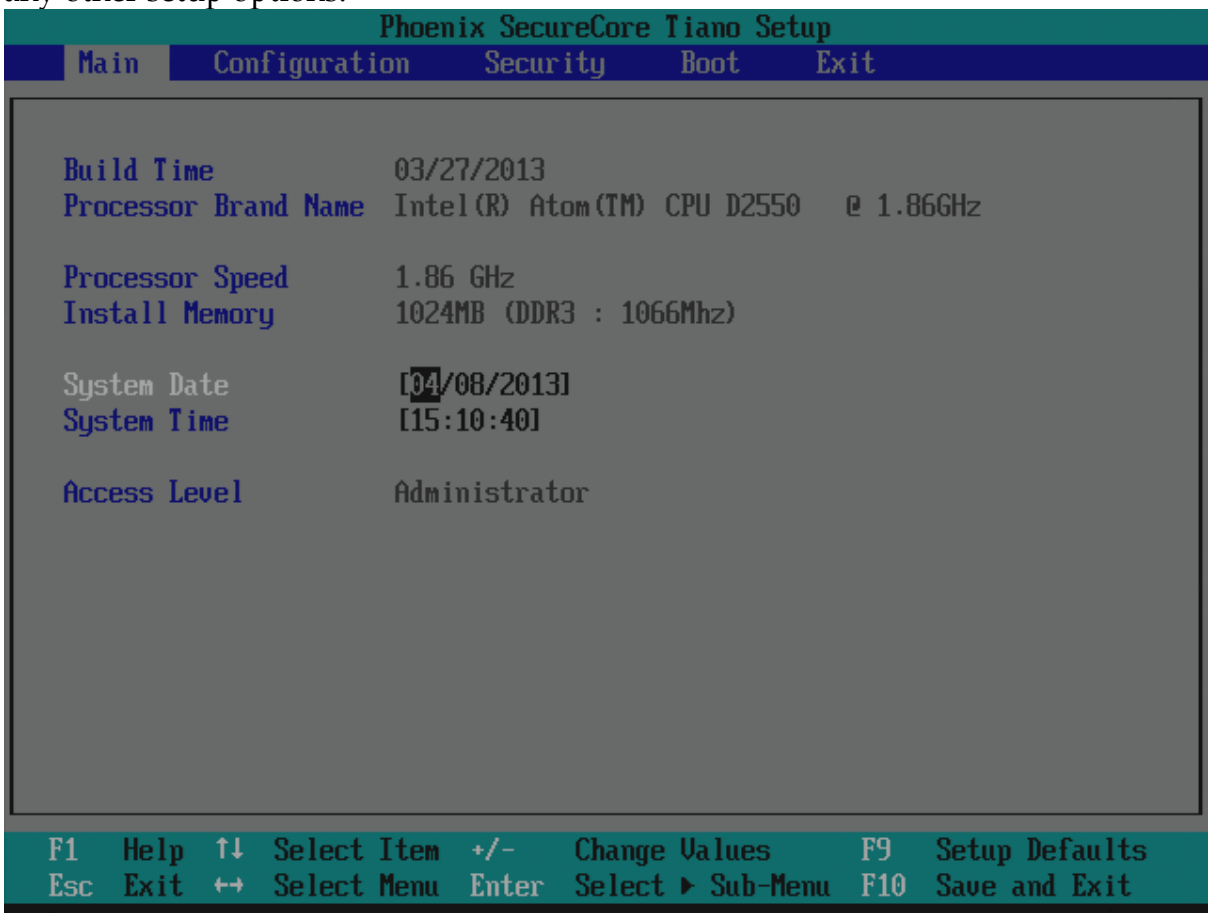
If the message disappears before you respond, but you still wish to enter Setup, please restart the system to try "COLD START" again by turning it OFF and then ON, or touch the "RESET" button. You may also restart from "WARM START" by pressing <Ctrl>, <Alt>, and <Delete> keys simultaneously. If you do not press the keys at the right time and the system will not boot, an error message will be displayed and you will again be asked to, Press <F2> to Run SETUP or Resume.
In HIFLEX BIOS setup, you can use the keyboard to choose among options or modify the system parameters to match the options with your system. The table below will show you all of keystroke functions in BIOS setup.



4.2 Main

Once you enter NANO-5050 Phoenix BIOS CMOS Setup Utility, a Main Menu is presented. The Main Menu allows user to select from eleven setup functions and two exit choices. Use arrow keys to switch among items and press <Enter> key to accept or bring up the sub-menu.

This setup page includes all the items in standard compatible BIOS. Use the arrow keys to highlight the item and then use the <PgUp>/<PgDn> or <+>/<-> keys to select the value or number you want in each item and press <Enter> key to certify it. Follow command keys in CMOS Setup table to change Date, Time, Drive type and any other setup options.



System Time

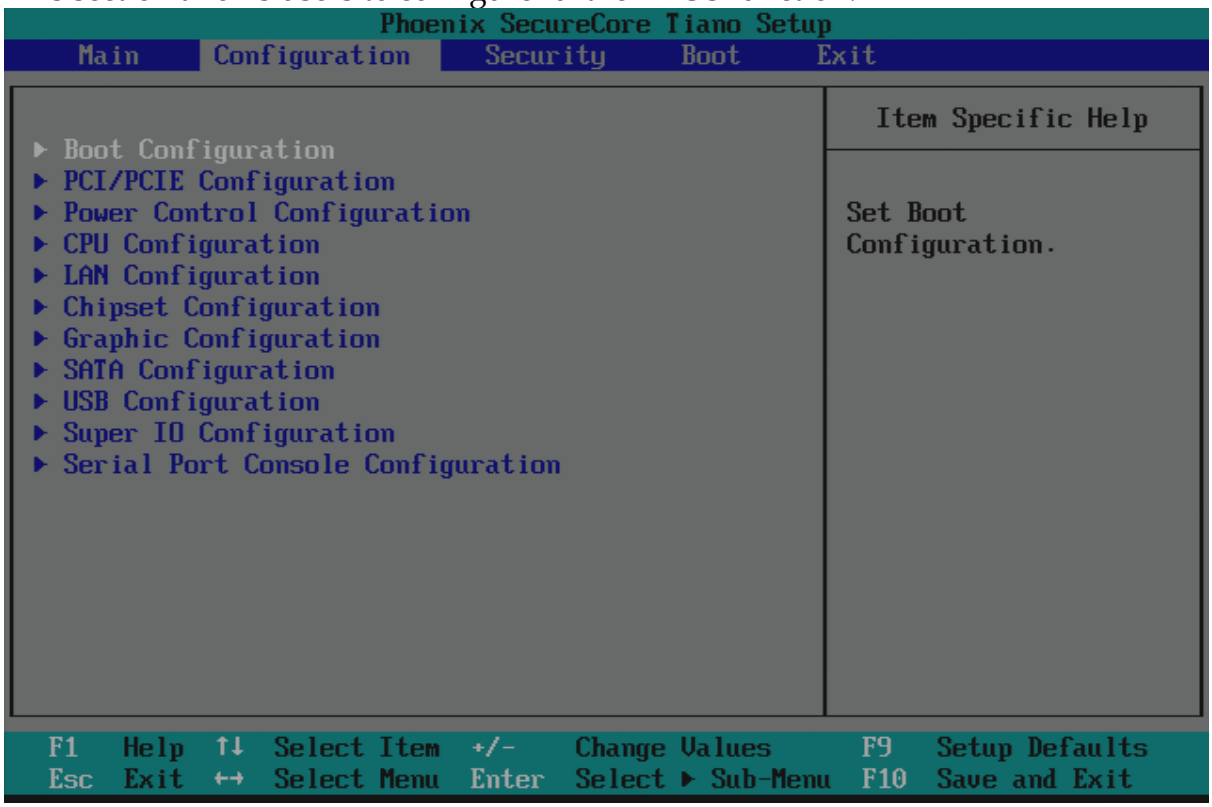
The time format is <Hour> <Minute> <Second>. Use [+] or [−] to configure system Time.

System Date

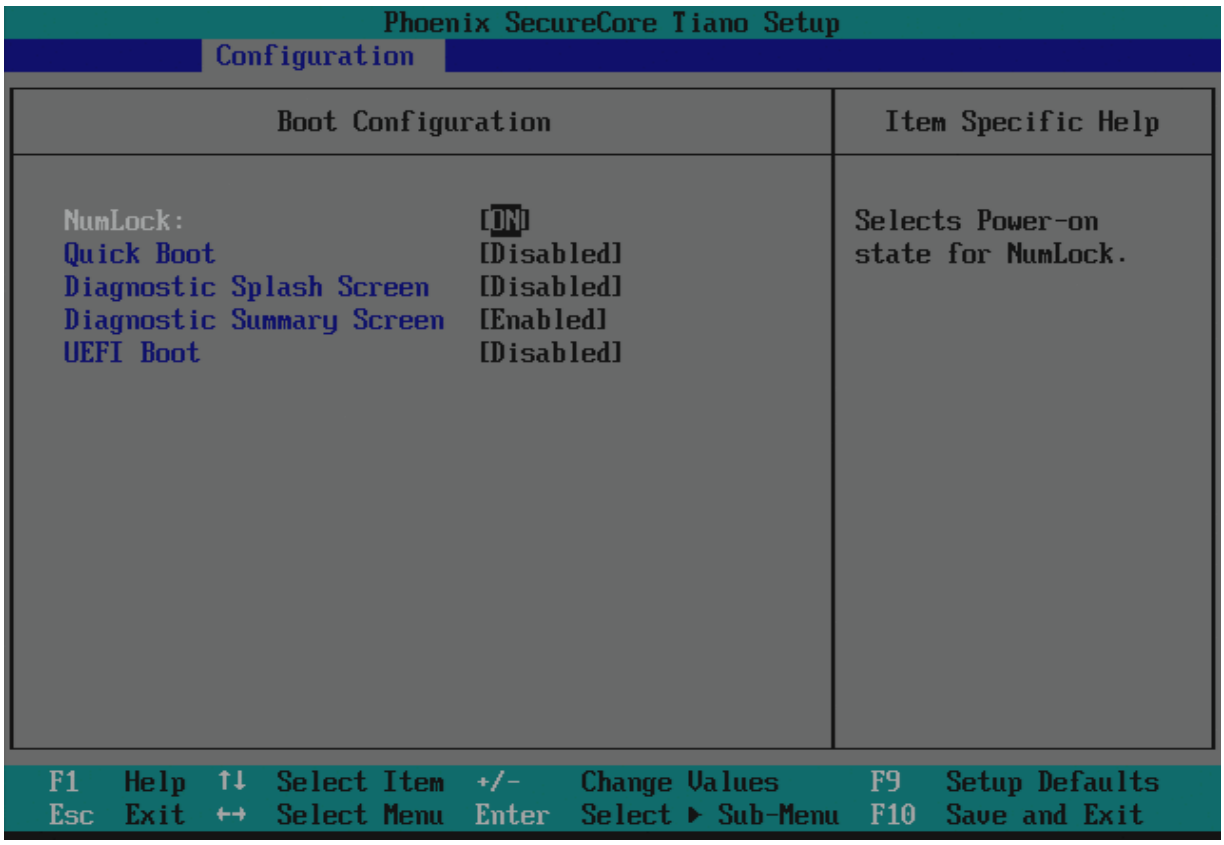
The date format is <Day>, <Month> <Date> <Year>. Use [+] or [−] to configure system Date.

4.3 Configuration

This section allows users to configure further BIOS function.



Boot Configuration



NumLock:
Selects Power-on state for NumLock.
Choices: Off, On

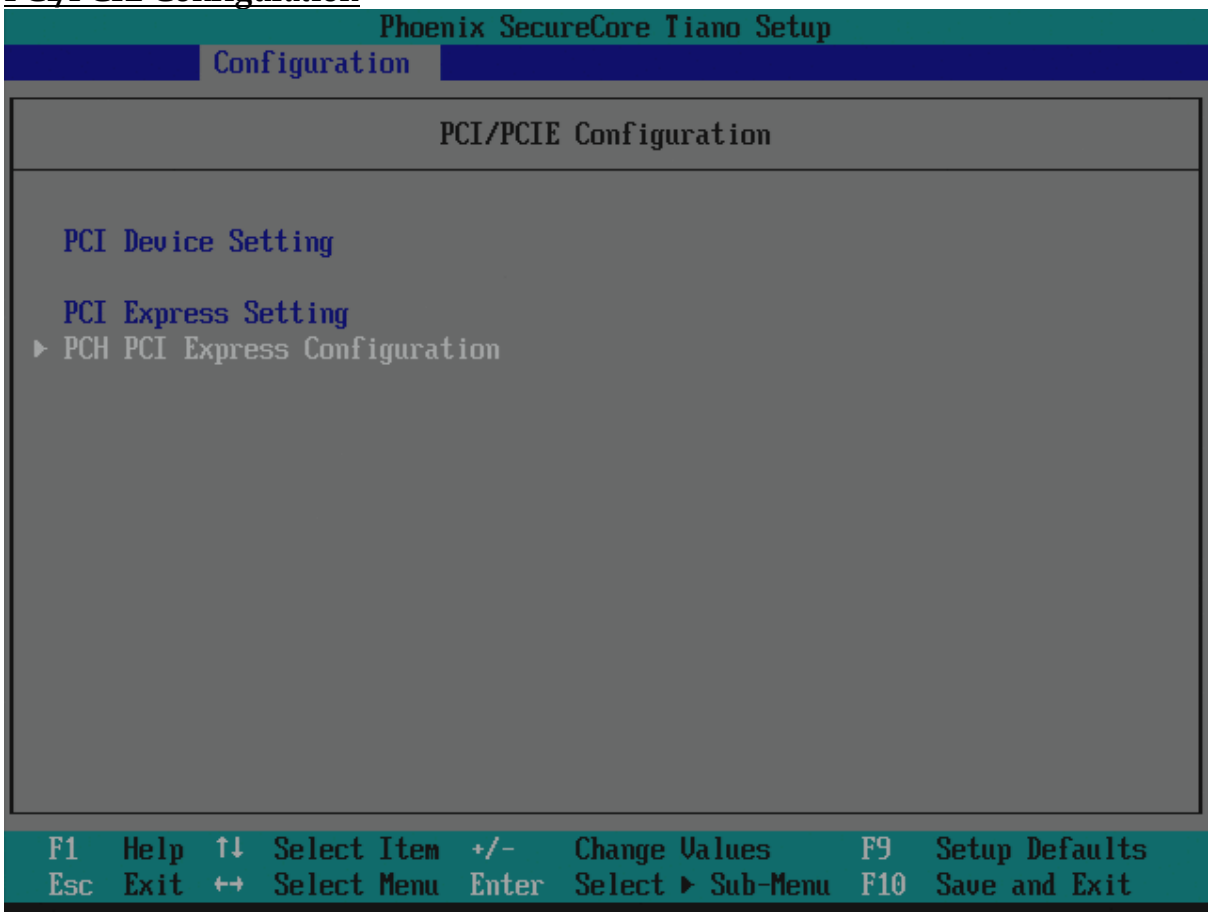
Quick Boot
Enable/Disable quick boot.
Choices: Enabled, Disabled

Diagnostic Splash Screen
If you select 'Enable' the diagnostic splash screen always display during boot. If you select 'Disabled' the diagnostic splash screen dose not display unless you press HOTKEY during boot.
The choice: Enabled, Disabled.

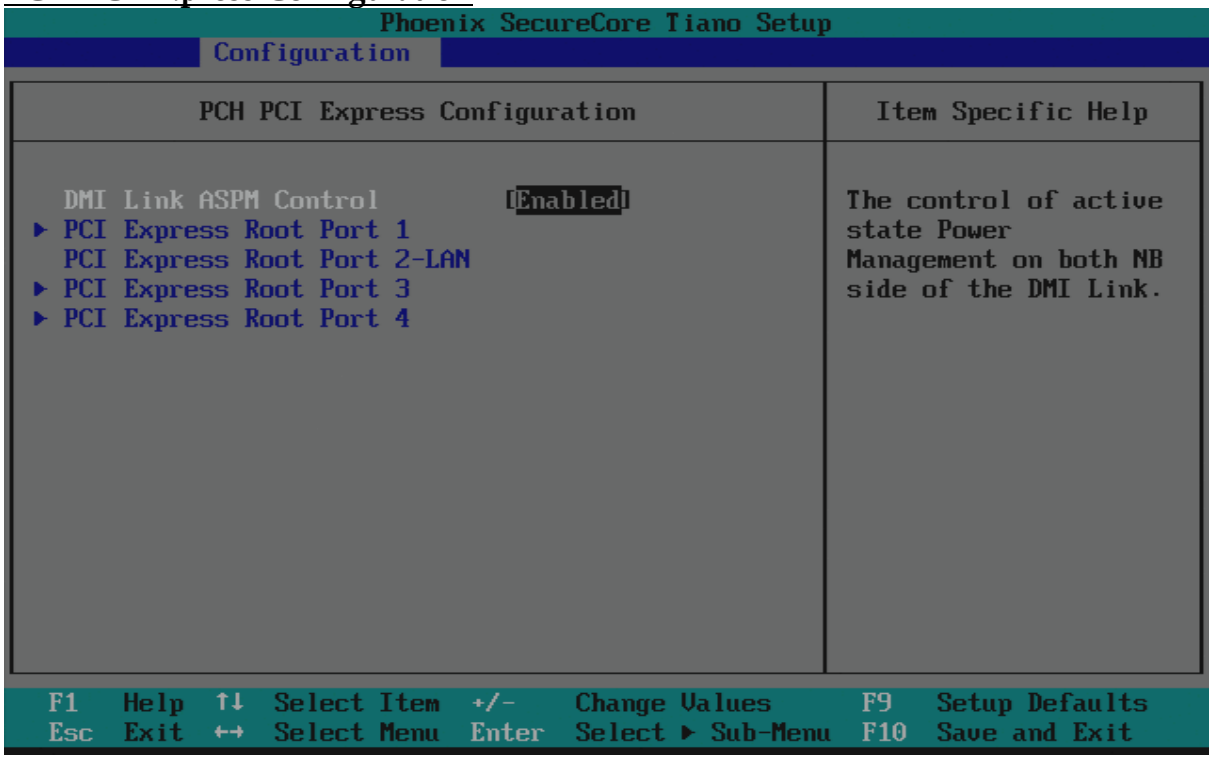
Diagnostic Summary Screen
Display the Diagnostic summary screen during boot.
The choice: Enabled, Disabled.

UEFI Boot
Enables the UEFI Boot.
The choice: Enabled, Disabled.

PCI/PCIE Configuration



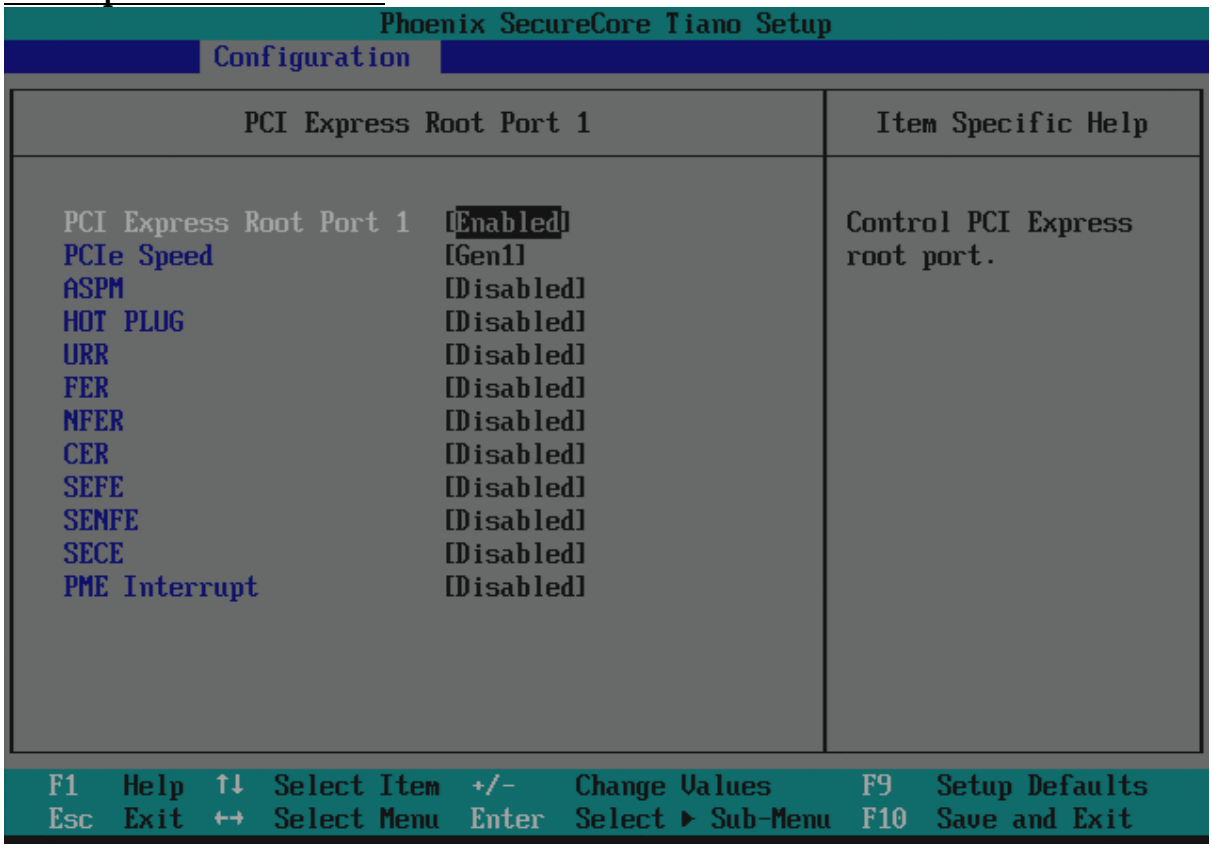
PCH PCI Express Configuration



DMI Link ASPM Control

The control of active state Power Management on both NB side of the DMI Link.
Choices: Enabled, Disabled.

PCI Express Root Port 1~4



PCI Express Root Port 1/2/3/4
Control the PCI Express Root Port.

PCIe Speed
Select PCIe Speed to Gen1 or Gen2 .

ASPM
Control PCIe Active State Power Management settings.
configure : Disable, L0S, L1, L0S And L1, Auto

HOT PLUG
Enable or disable PCI Express Hot Plug.

URR
Enable or disable PCI Express Unsupported Request Reporting.

FER
Enable or disable PCI Express Device Fatal Error Reporting.

NFER
Enable or disable PCI Express Device Non-Fatal Error Reporting.

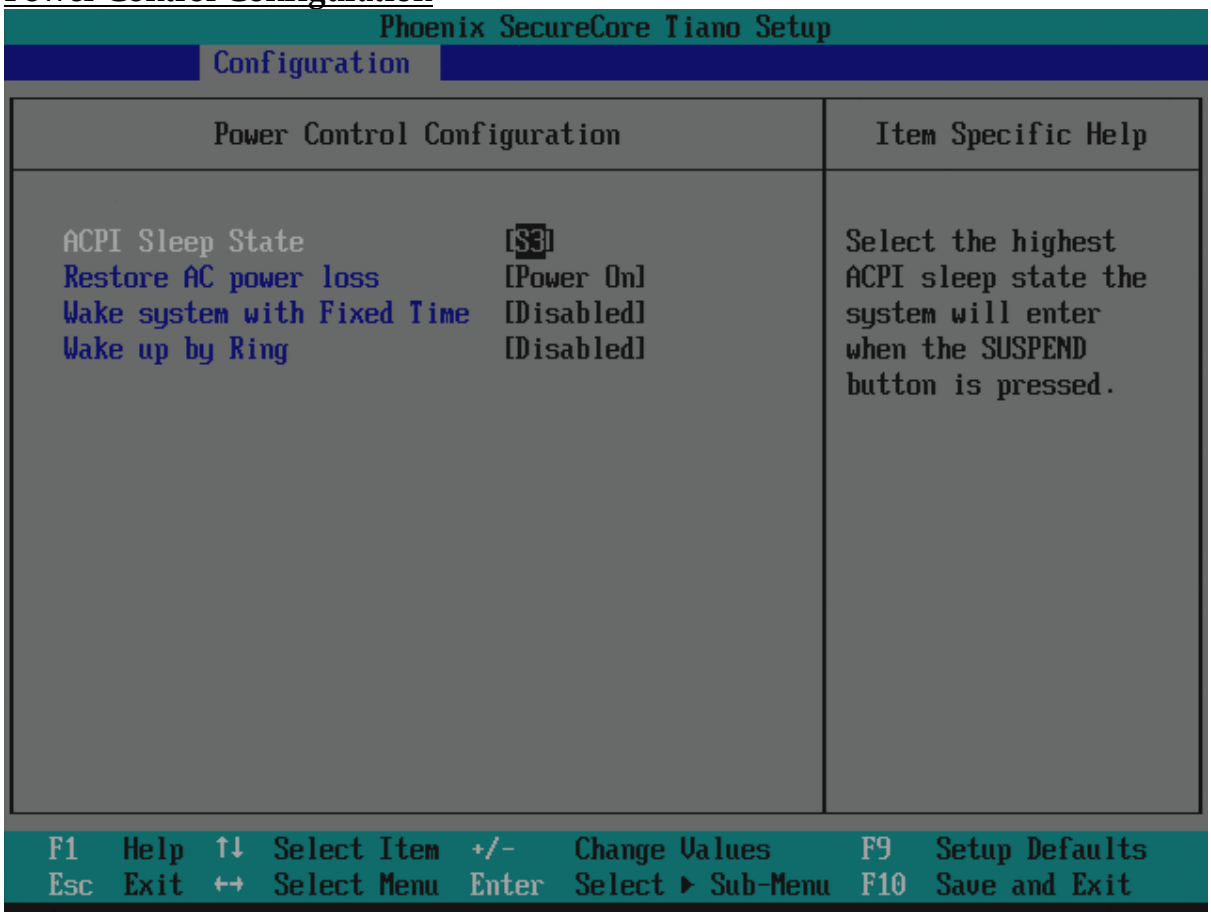
CER
Enable or disable PCI Express Device Correctable Error Reporting.
SEFE
Enable or disable Root PCI Express System Error on Fatal Error.

SENFE
Root PCI Express System Error on Non-Fatal Error Enable/Disable.

SECE
Root PCI Express System Error on Correctable Error Enable/Disable.

PME Interrupt
Root PCI Express PME Interrupt Enable/Disable.

Power Control Configuration



ACPI Sleep State

Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
The choice: S1 (CPU Stop Clock), S3 (Suspend to RAM)

Restore AC power loss

Select AC Power state when power is re-applied after a power failure.
The choice: Power Off, Power On, Last State.

The choice: Disabled, Enabled.

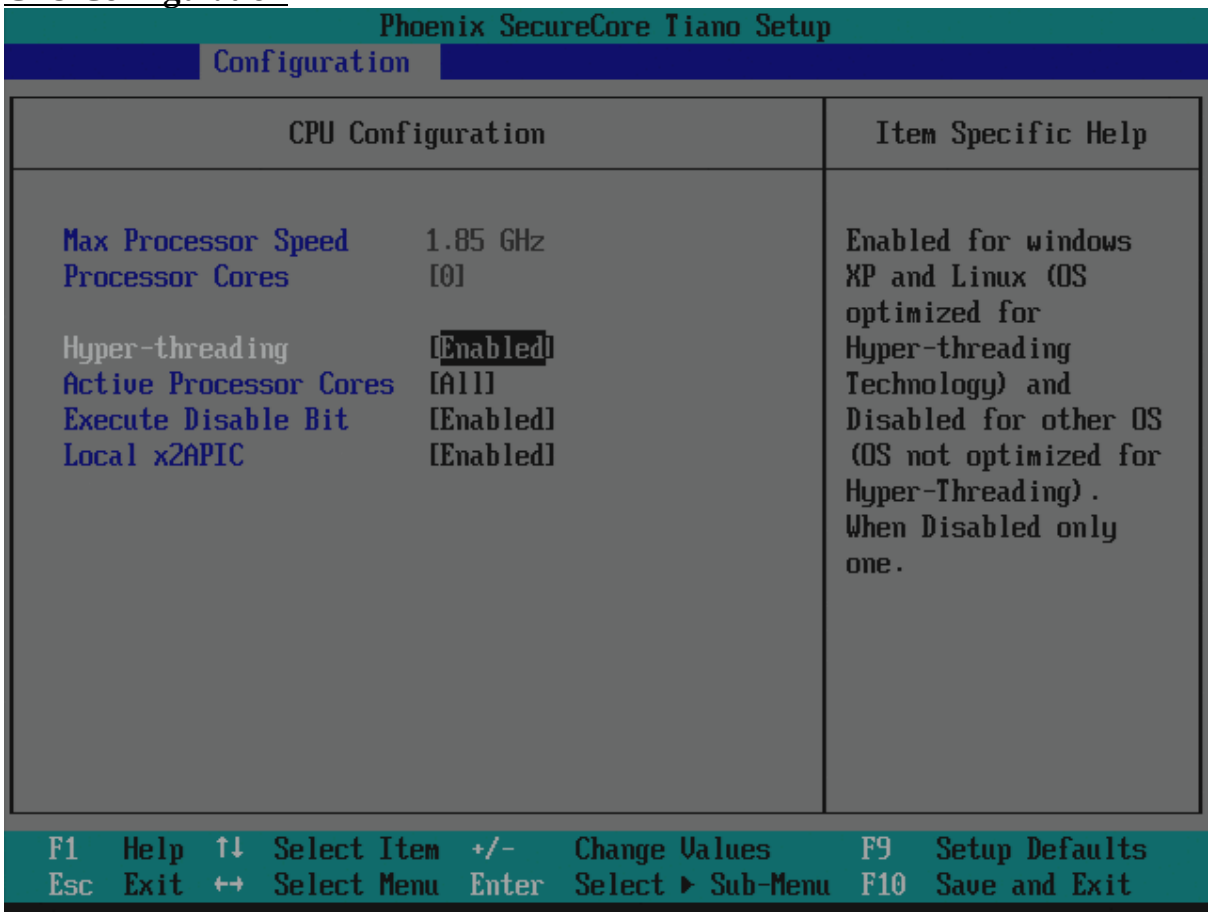
Wake System With Fixed Time

Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified.
Choices: Enabled, Disabled.

Wake up By Ring

Enable or disable Ring to wake the system.
Choices: Enabled, Disabled.

CPU Configuration



Hyper-threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper- Threading Technology). When Disabled only one.
Choices: Enabled, Disabled.

Active Processor Cores

Select the number of physical cores to enable in each processor package.
Choices: 1, All.

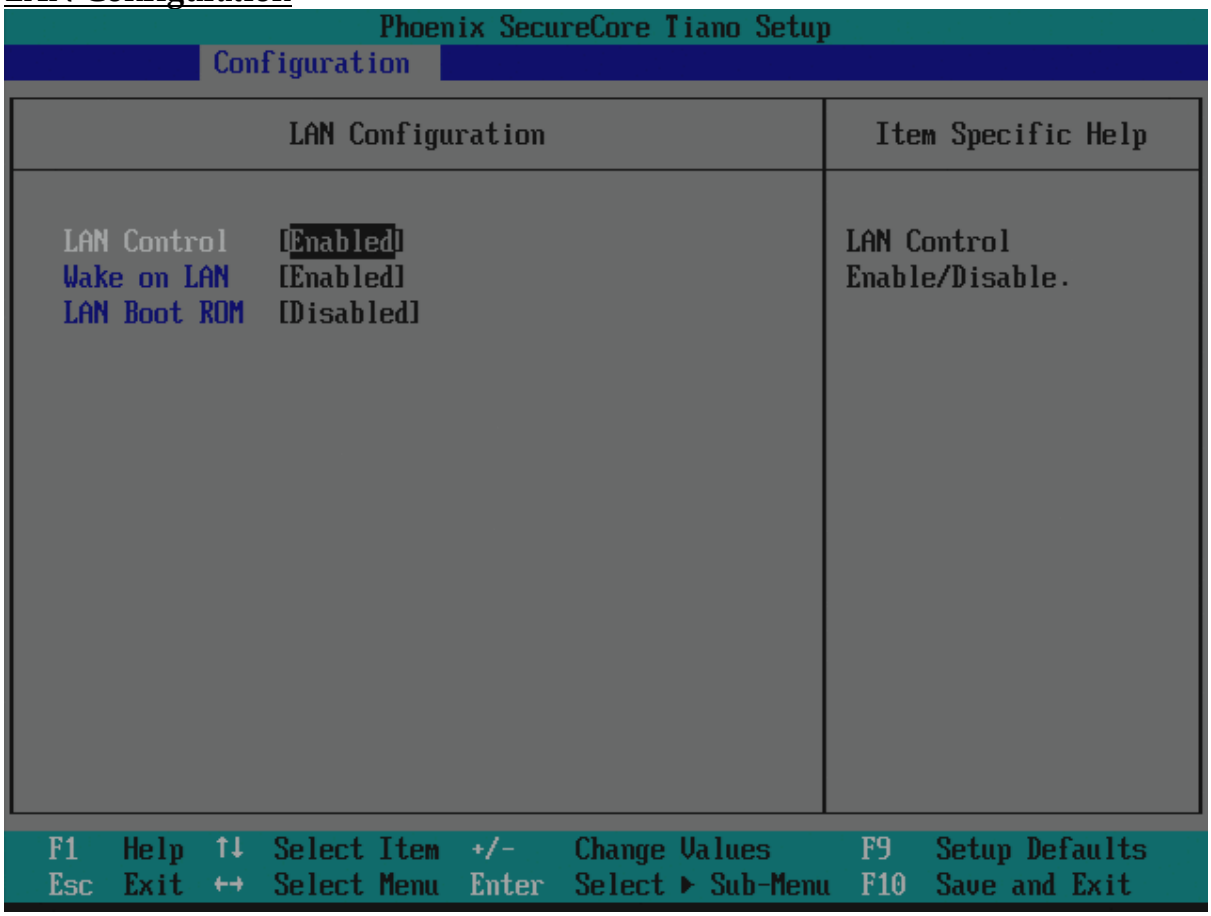
Execute Disable Bit

Enable Execute Disabled functionality. Also known as Data Execution Prevention (DEP).

Local x2APIC

Enable Local x2APIC. Some 0Ses do not support this.
Choices: Enabled, Disabled.

LAN Configuration



LAN Control

LAN Control Enabled/Disabled.
Choices: Enabled, Disabled.

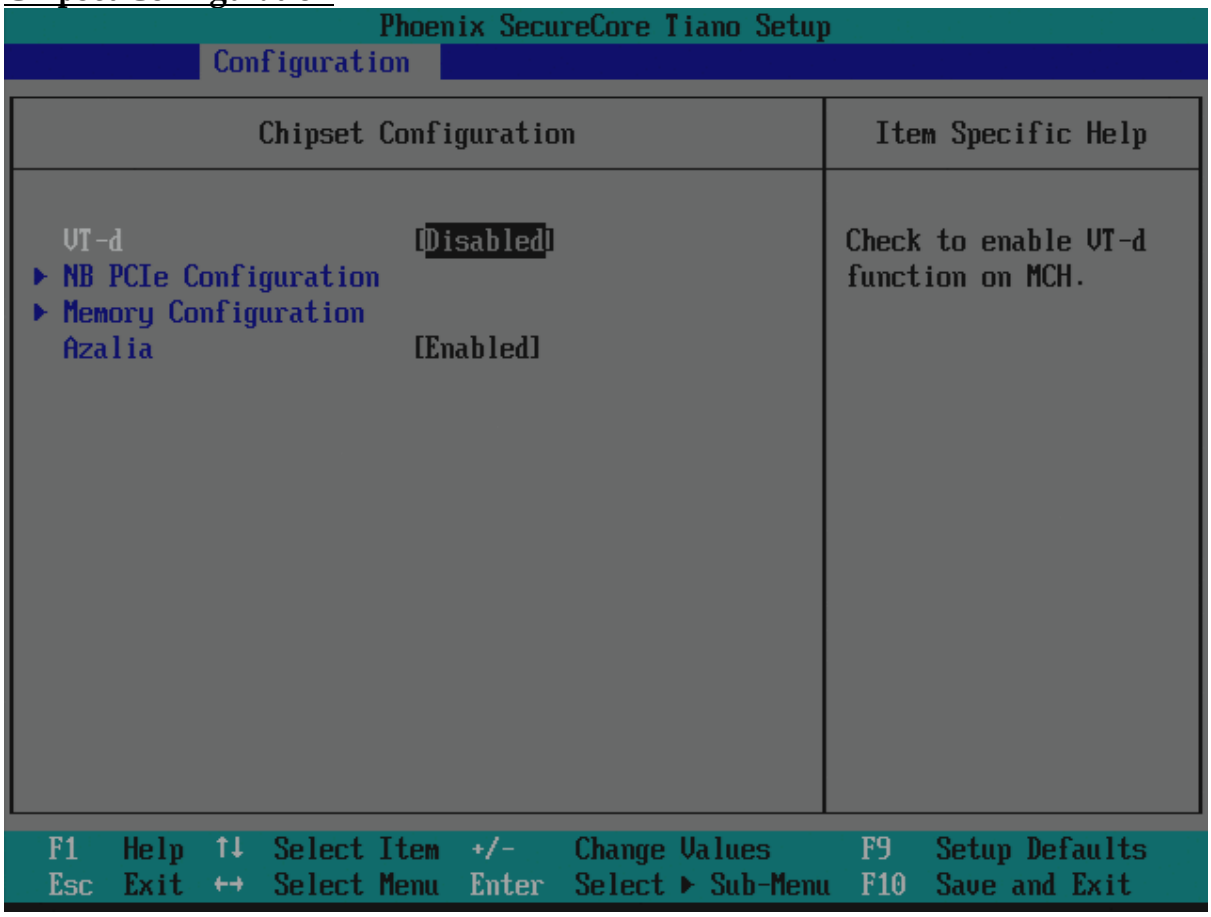
Wake on LAN

Enable or disable integrated LAN to wake the system.
Choices: Enabled, Disabled.

LAN Boot ROM

Enable or disable integrated LAN Boot ROM(PXE) function.
Choices: Enabled, Disabled.

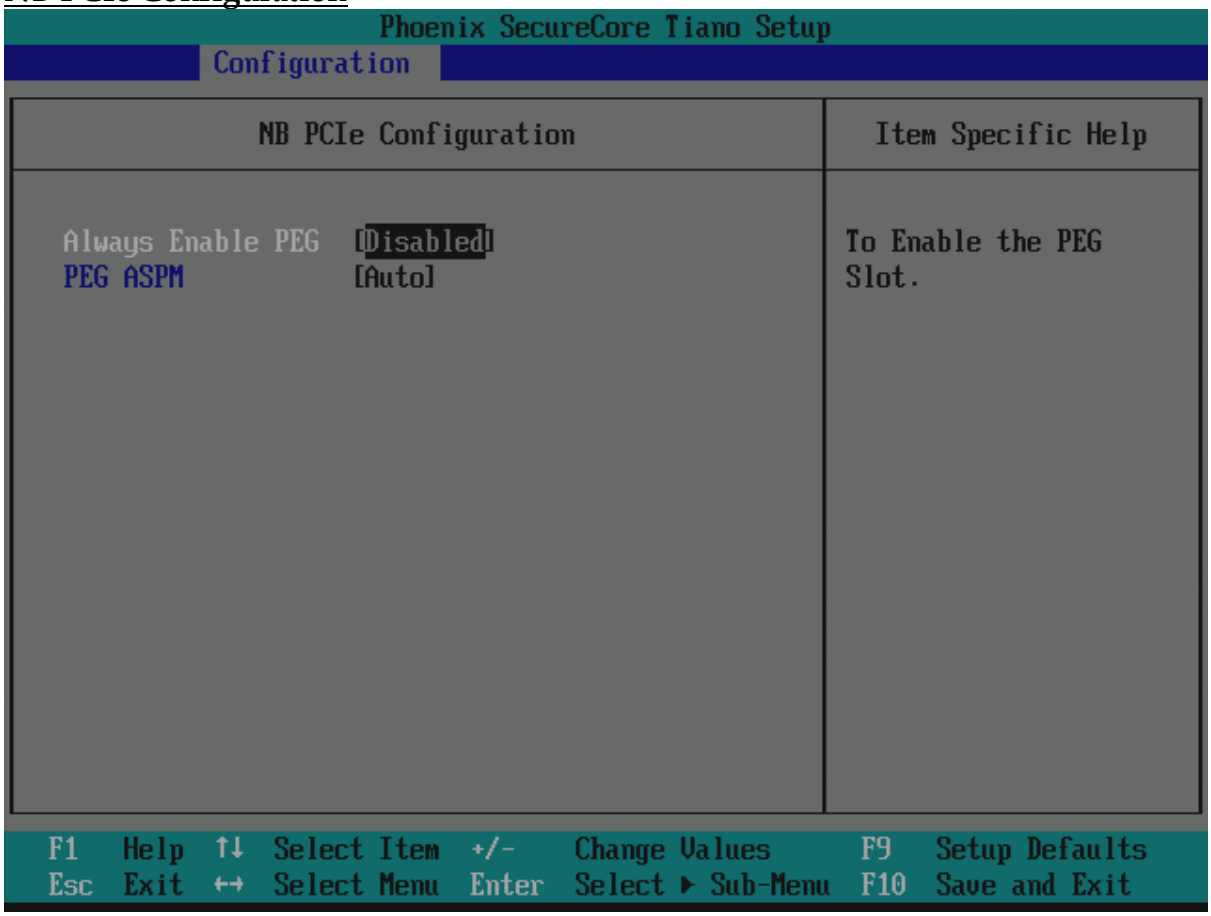
Chipset Configuration



VT-d
Check to enable VT-d function on MCH.
Choices: Enabled, Disabled.

Azalia
Control Detection of the Azalia device.
Choices: Enabled, Disabled.

NB PCIe Configuration



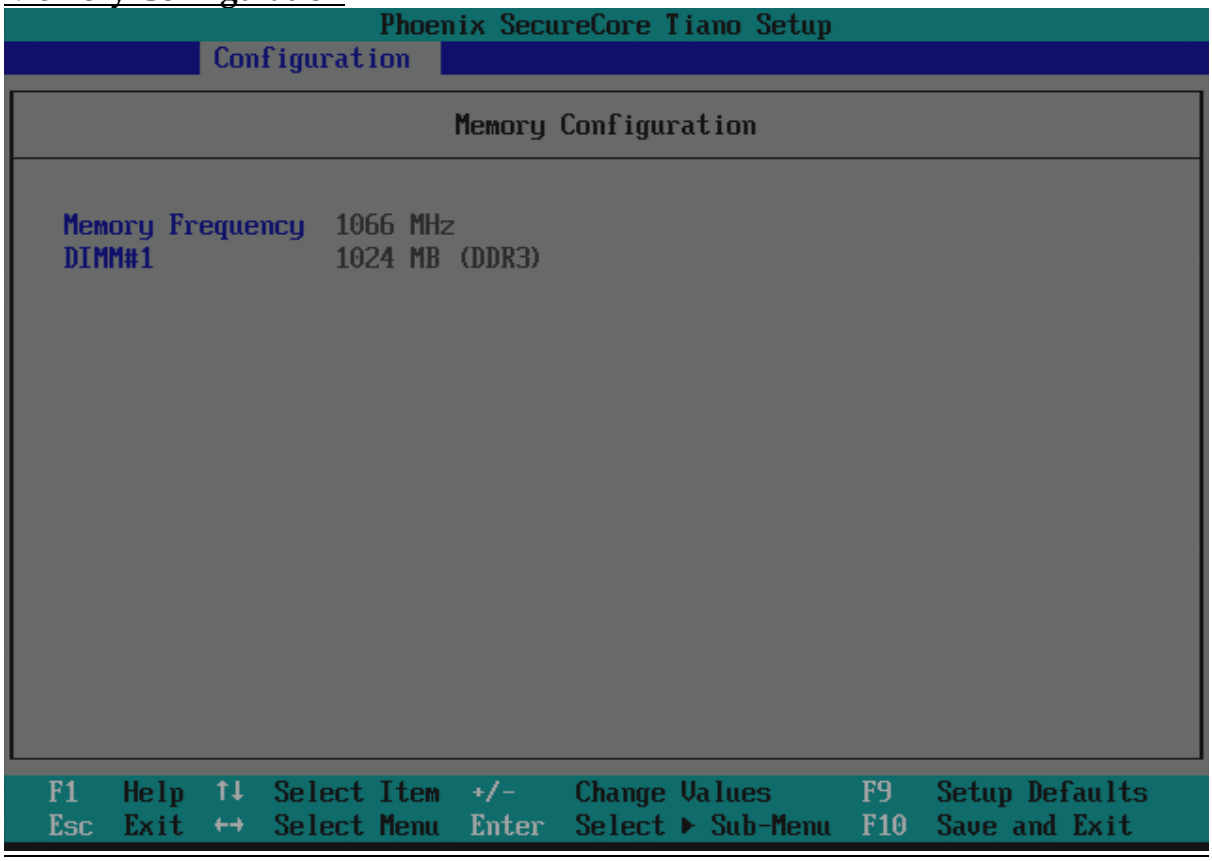
Always Enable PEG

To Enable the PEG Slot.
Choices: Enabled, Disabled.

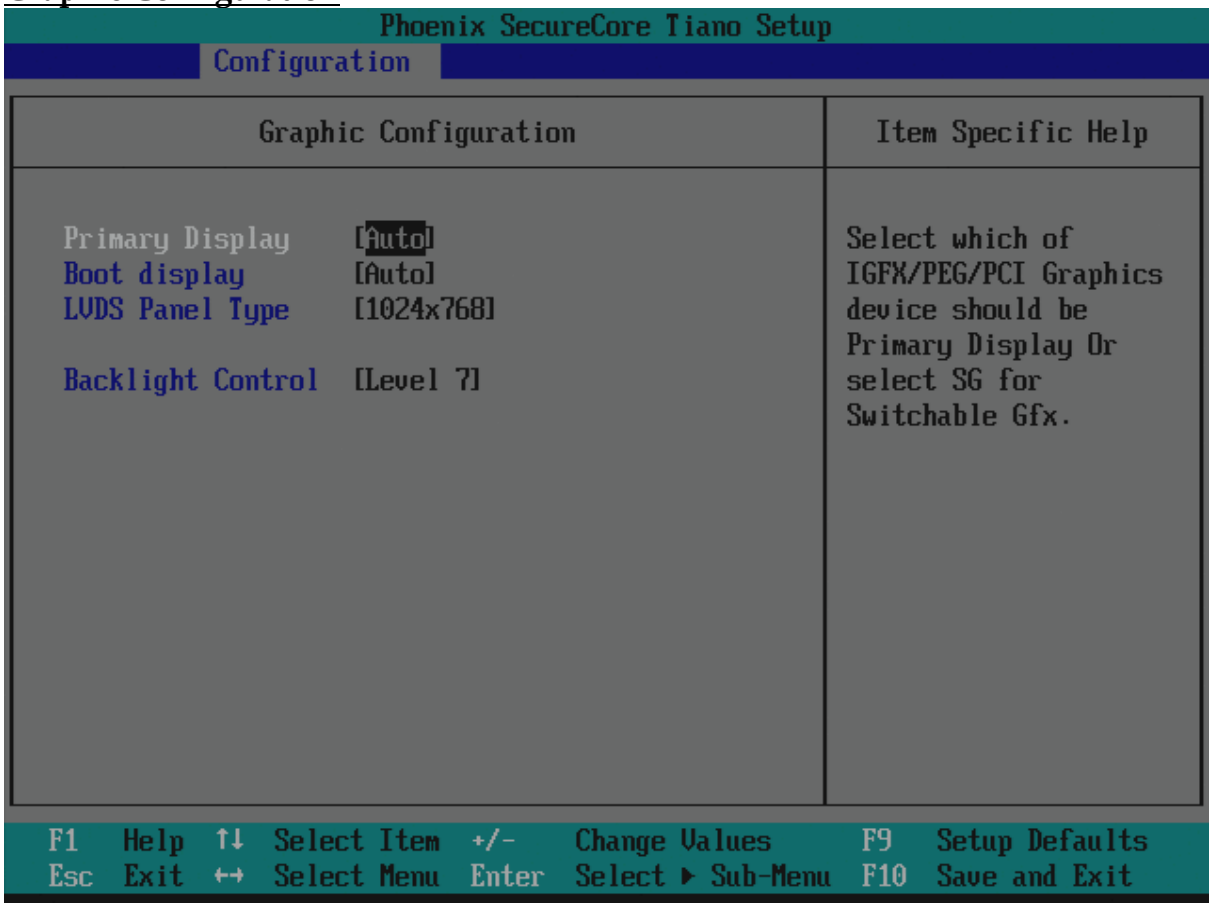
PEG ASPM

Control ASPM Support for the PEG Device. This has mp effect if PEF is not the current active device.
Choices: Disabled, Auto, ASPM L0s, ASPM L1, ASPM L0sL1.

Memory Configuration



Graphic Configuration



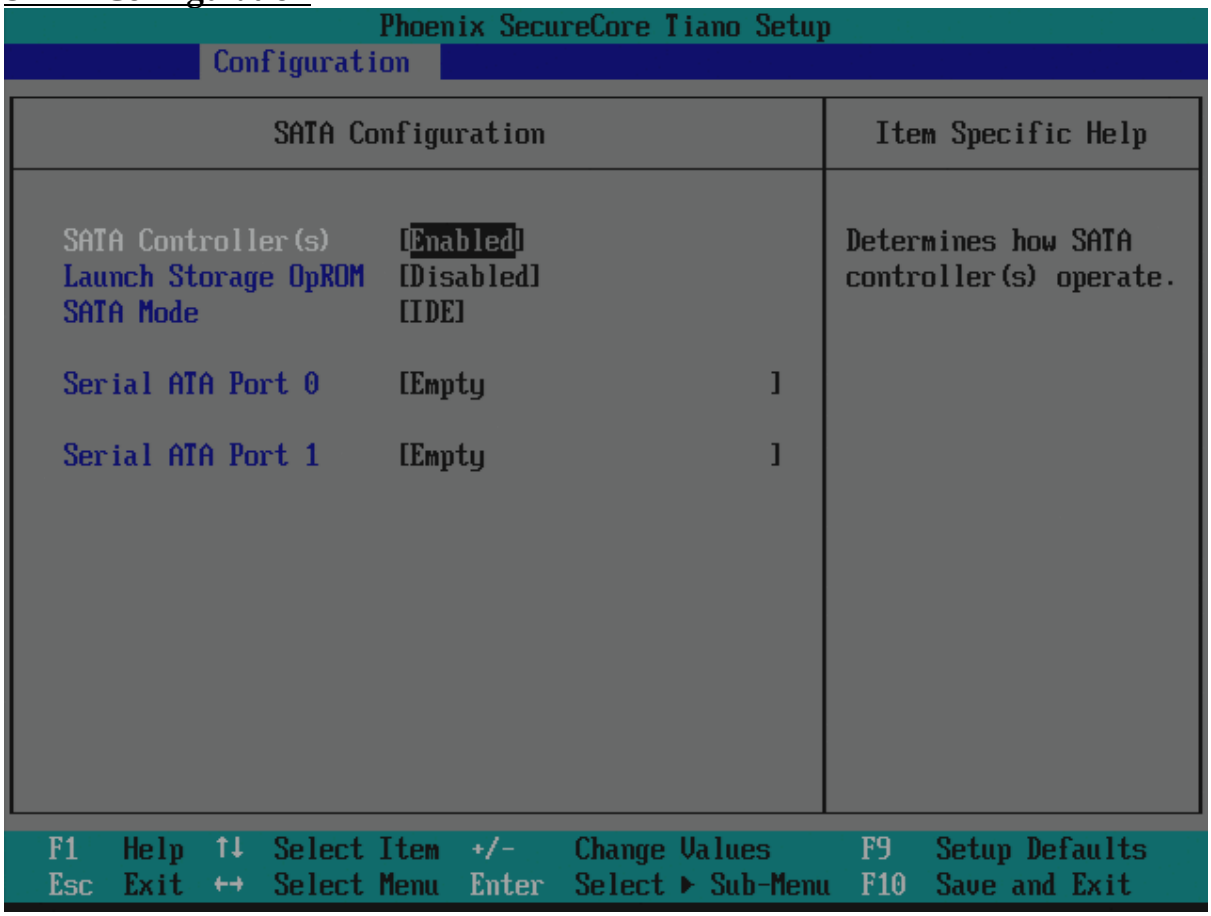
Primary Display
Select which of IGFX/PEG/PCI Graphics device should be Primary Display or select SG for Switchable Gfx.
The choice: Auto, IGFX, PEG.

Boot Display
Select the video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.
Choices: Auto, CRT, DP, LVDS, CRT+LVDS, CRT+DP, LVDS + DP

LVDS Panel Type
Select LCD Panel used by internal Graphics by selecting the appropriate setup item.
Choices: 800x600, 1024x768, 1280x800, 1280x1024, 1920x1080

Backlight Control
Choices: Level 1, Level 2, Level 3, Level 4, Level 5, Level 6, Level 7.

SATA Configuration



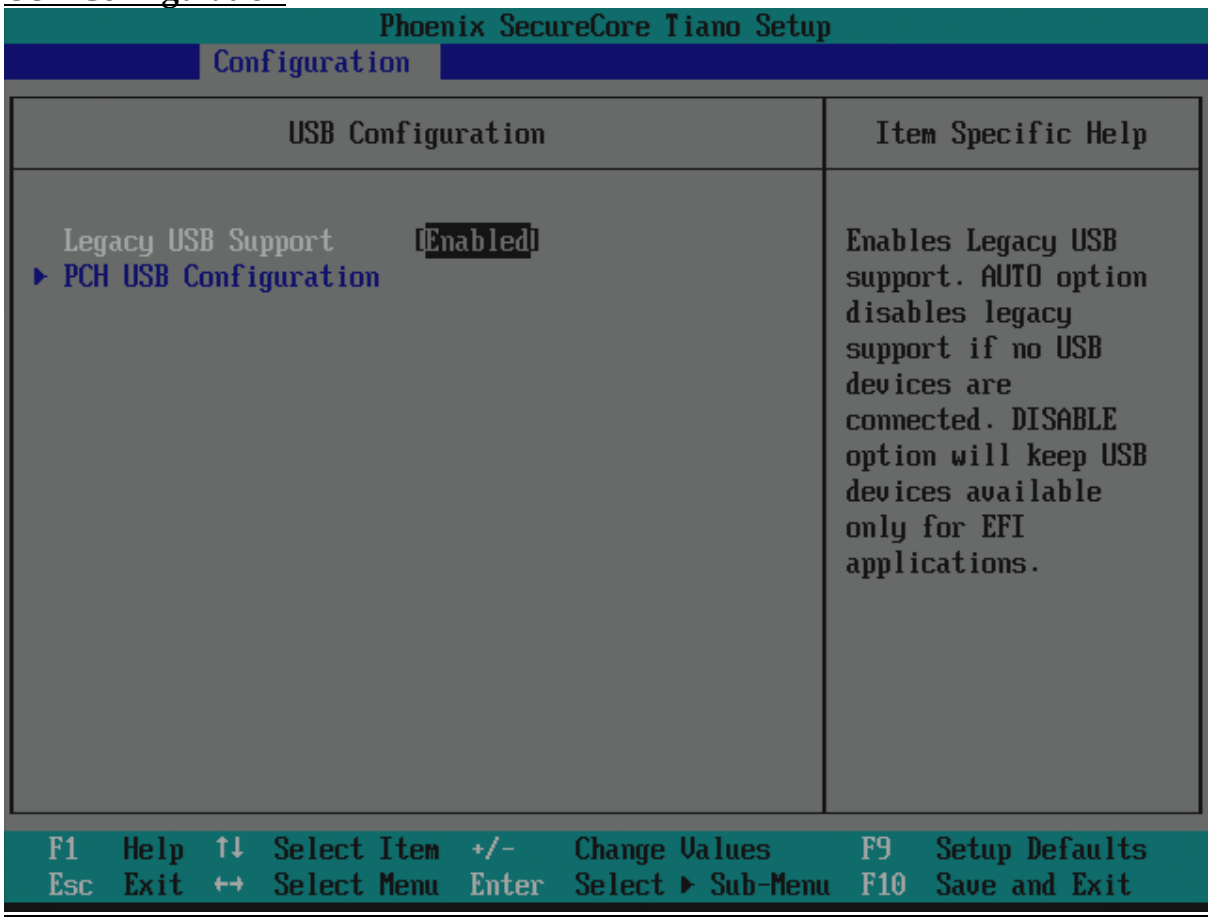
SATA Controller(s)
Determines how SATA controller(s) operate
Choices: Enabled, Disabled

Launch Storage OpROM
Enable or disable boot option Launch Storage devices with option ROM.
Choices: Enabled, Disabled.

SATA Mode
Determines how SATA controller(s) operate.
The choice: IDE, AHCI.

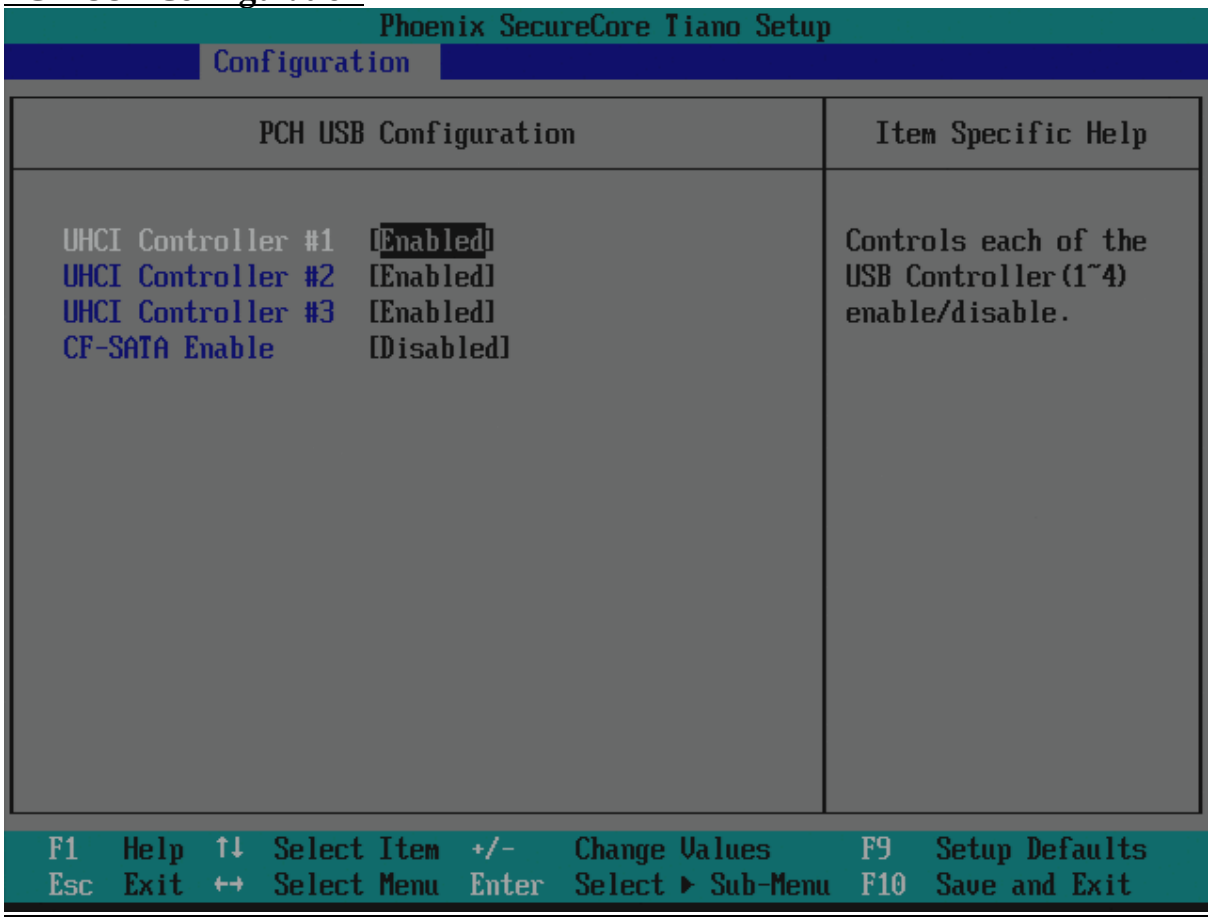
Serial ATA Port 0/1
Display the identity of the device attached.

USB Configuration



Legacy USB Support
Enable Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB device available only for EFI applications
Choices: Enabled Disabled.

PCH USB Configuration



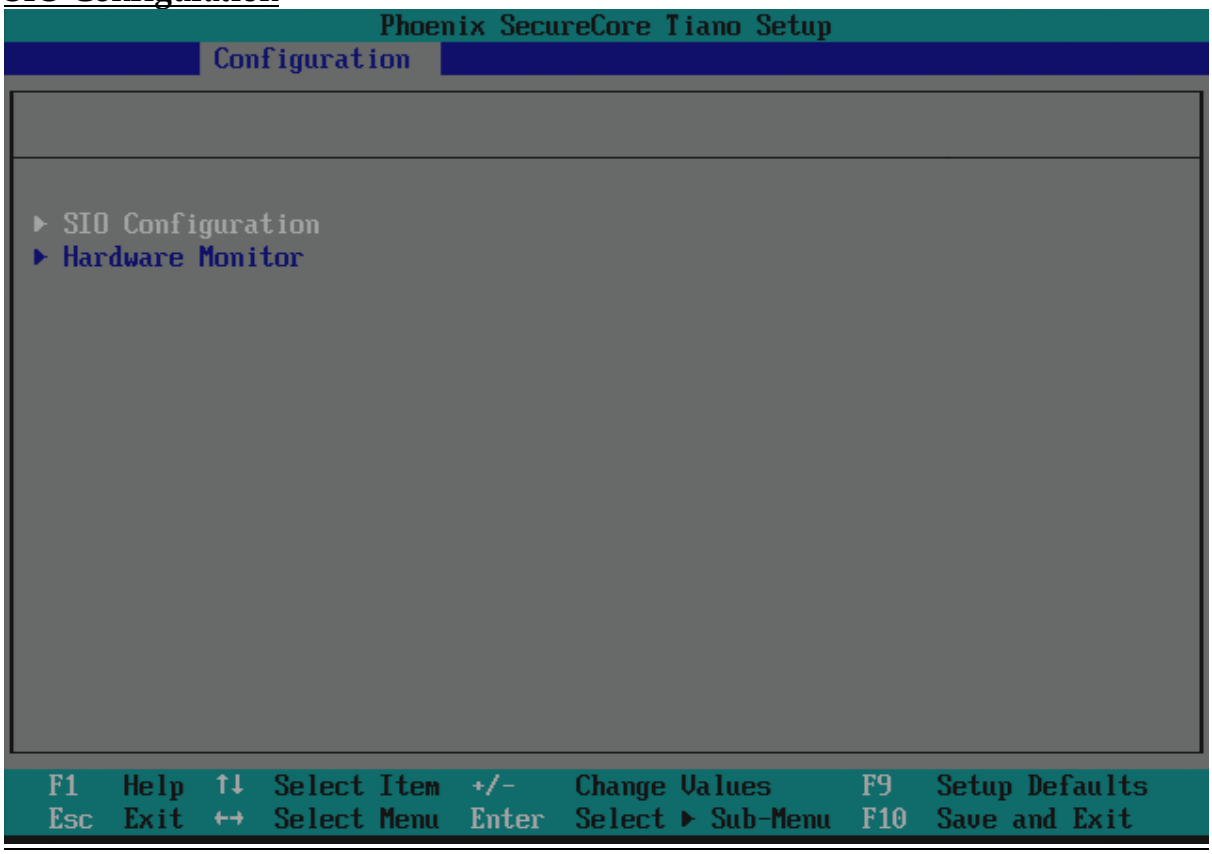
UHCI Controller #1~#3

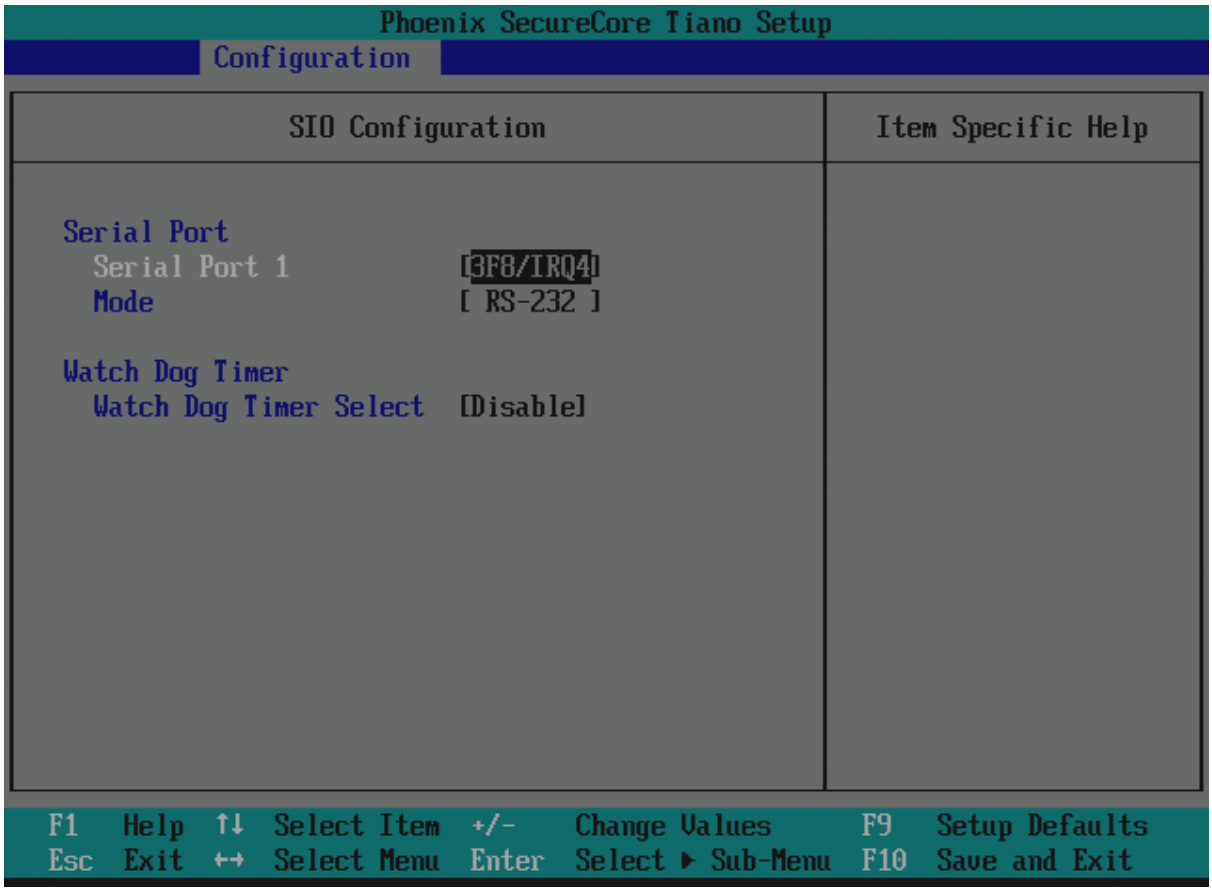
Control each of the USB Controller(1~4)
Choices: Enabled, Disabled

CF-SATA Enable

CF-SATA Enable/Disable.
Choices: Enabled, Disabled.

SIO Configuration



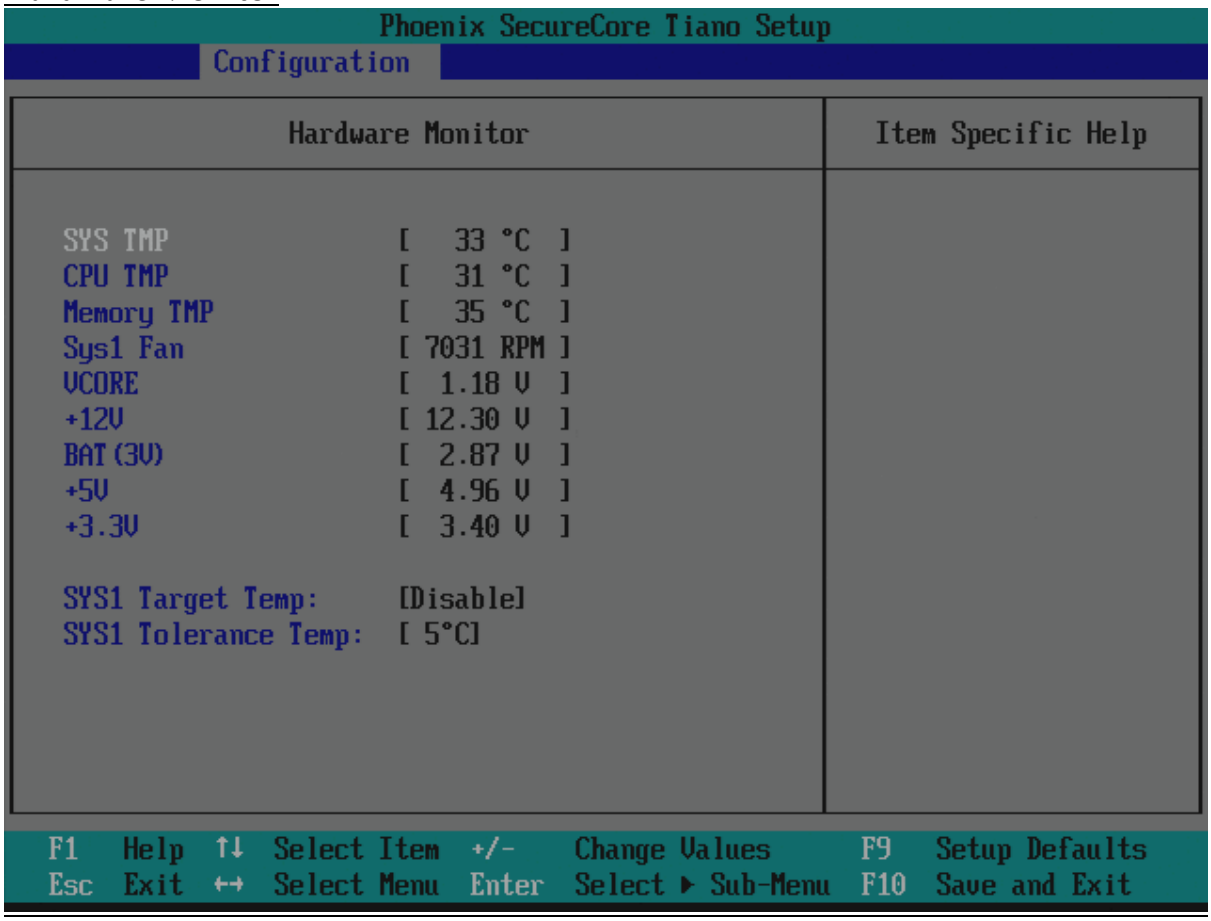


Serial Port 1
Choices: 3F8/IRQ4, 2F8/IRQ3, Disable.

Mode
Choices: RS-232, RS-422, RS-485.

Watch Dog Timer Select
Choices: Disable, 15secs, 30secs, 1min, 2mins, 3mins

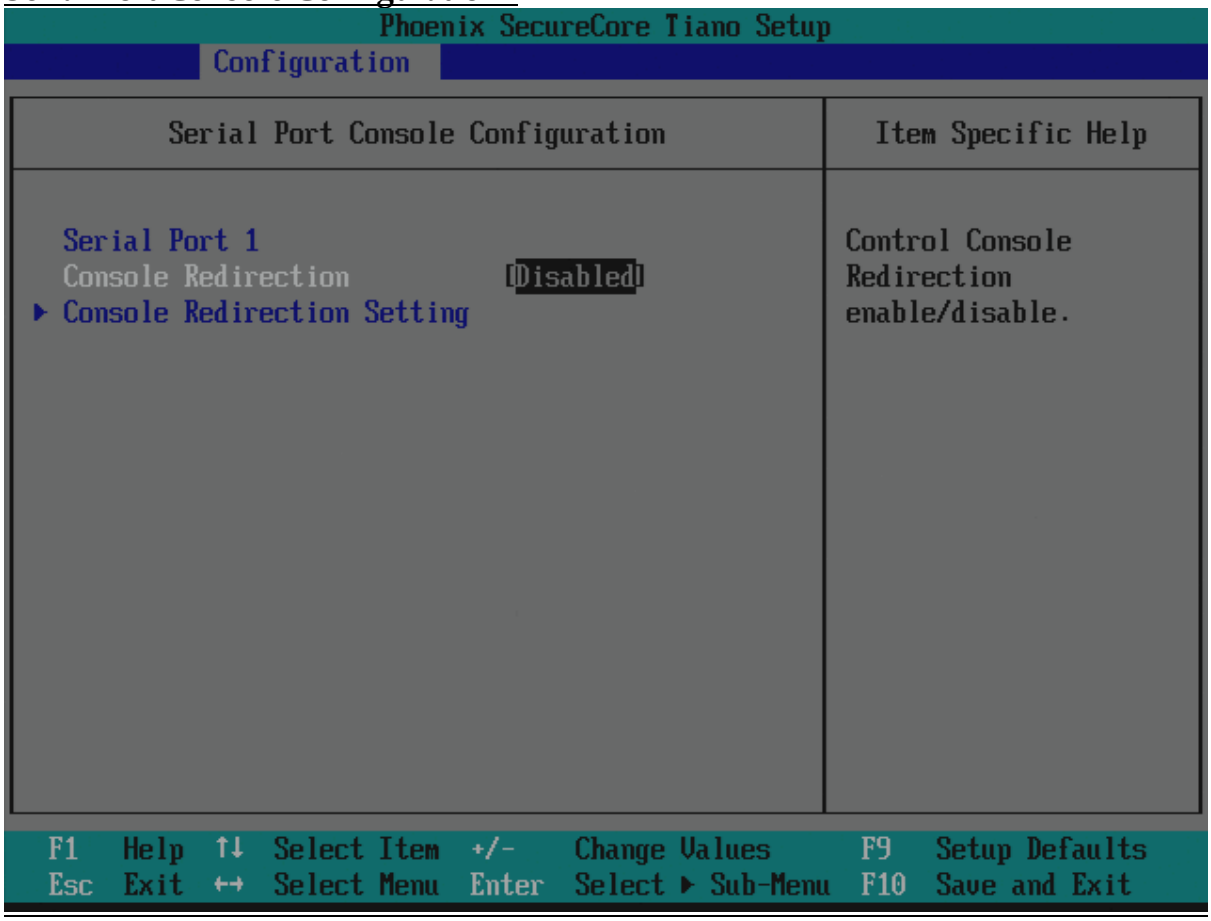
Hardware Monitor



SYS1 Target Temp:
SYS1 FAN Target Temperature
Choices: Disable, 40˚C, 45˚C, 50˚C, 55˚C.

SYS1 Tolerance Temp:
CPU FAN Tolerance Temperature
Choices: Disable, 5˚C, 4˚C, 3˚C, 2˚C, 1˚C.

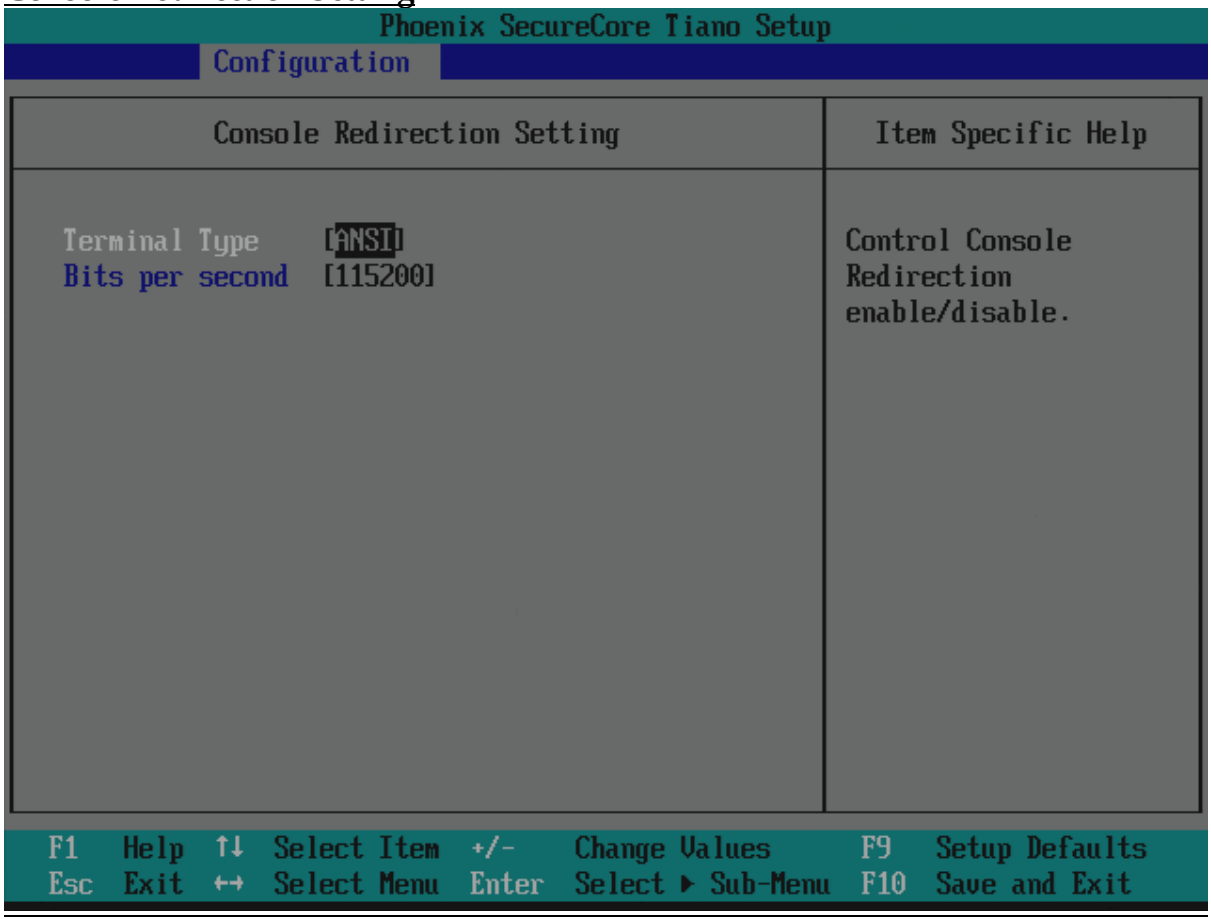
Serial Port Console Configuration



Console Redirection

Console Redirection Enable or Disable
Choices: Enabled, Disabled

Console Redirection Setting



Terminal Type

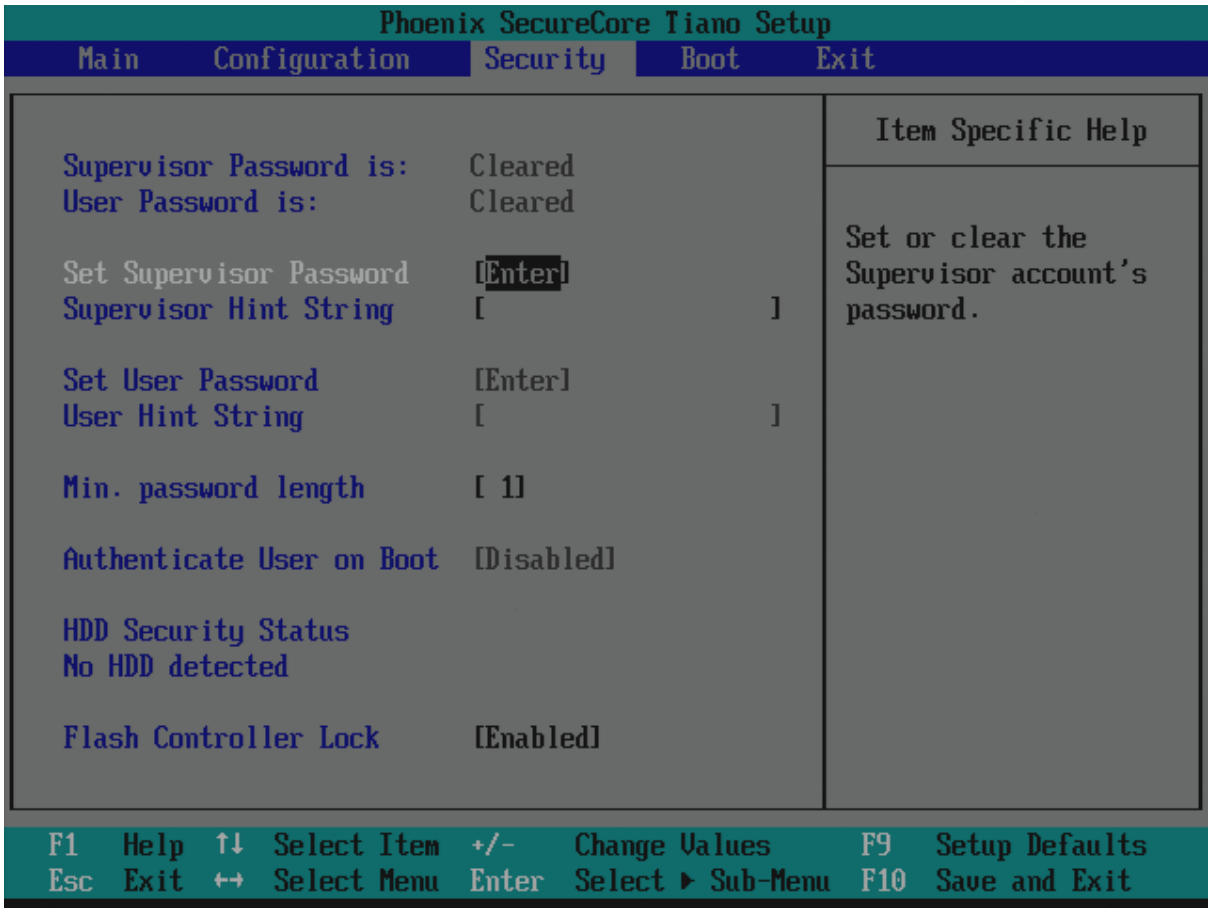
VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in console Redirection Settings page, for more Help with Terminal Type/Emulation.
The choice: VT100, VT100+, VT-UTF8, ANSI

Bits Per second

Select serial port transmission speed
The choice: 9600, 19200, 57600, 115200.

4.4 Security

This section lets you set security passwords to control access to the system at boot time and/or when entering the BIOS setup program. Some systems have a single password, while many newer ones now have two: a supervisor and a user password.



Set Supervisor Password
Set or Clear Supervisor Password

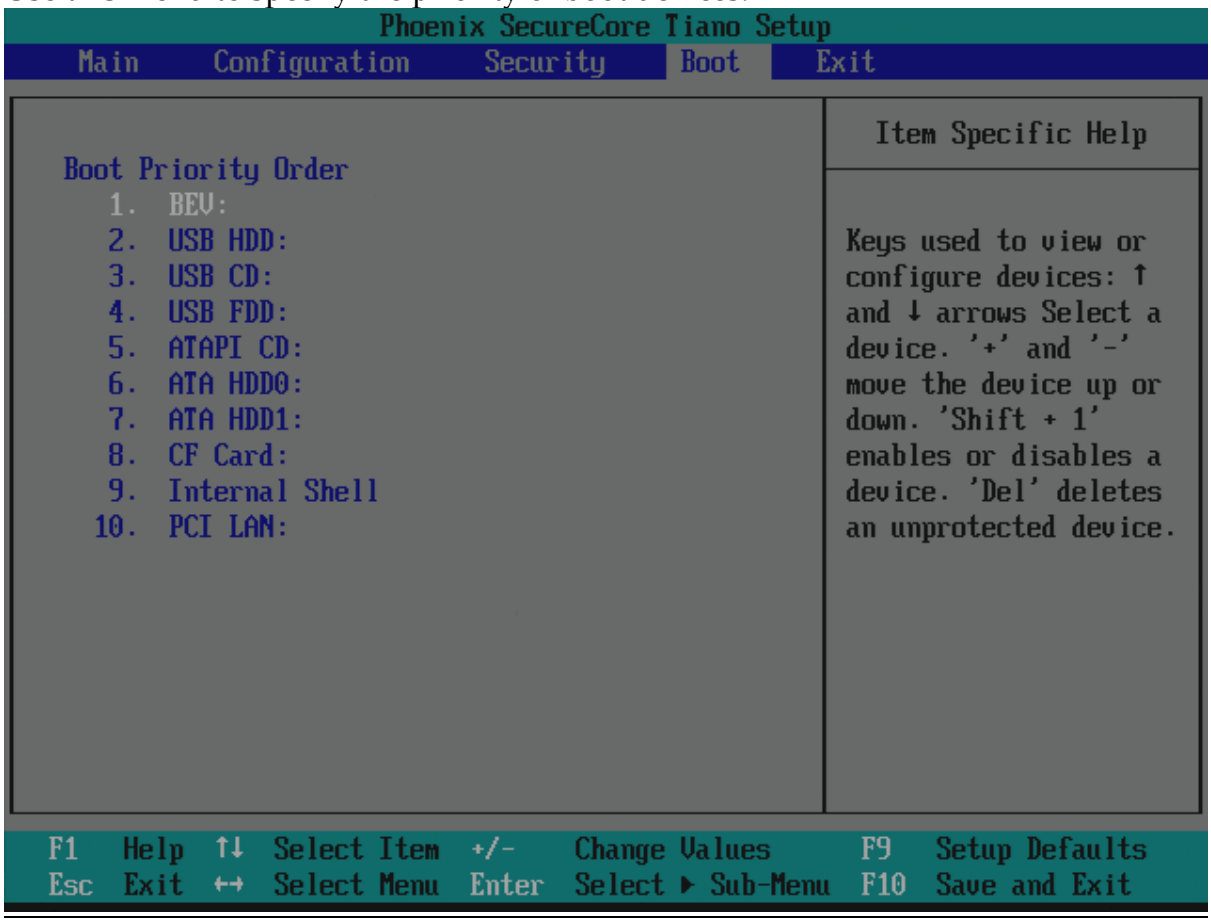
Supervisor Hint String
Press Enter to type Supervisor Hint String

Min. password length
Set the minimum number of characters for password (1-20).

Flash Controller Lock
Lock all flash controllers
The choice: Enabled, Disabled.

4.5 Boot

Use this menu to specify the priority of boot devices.



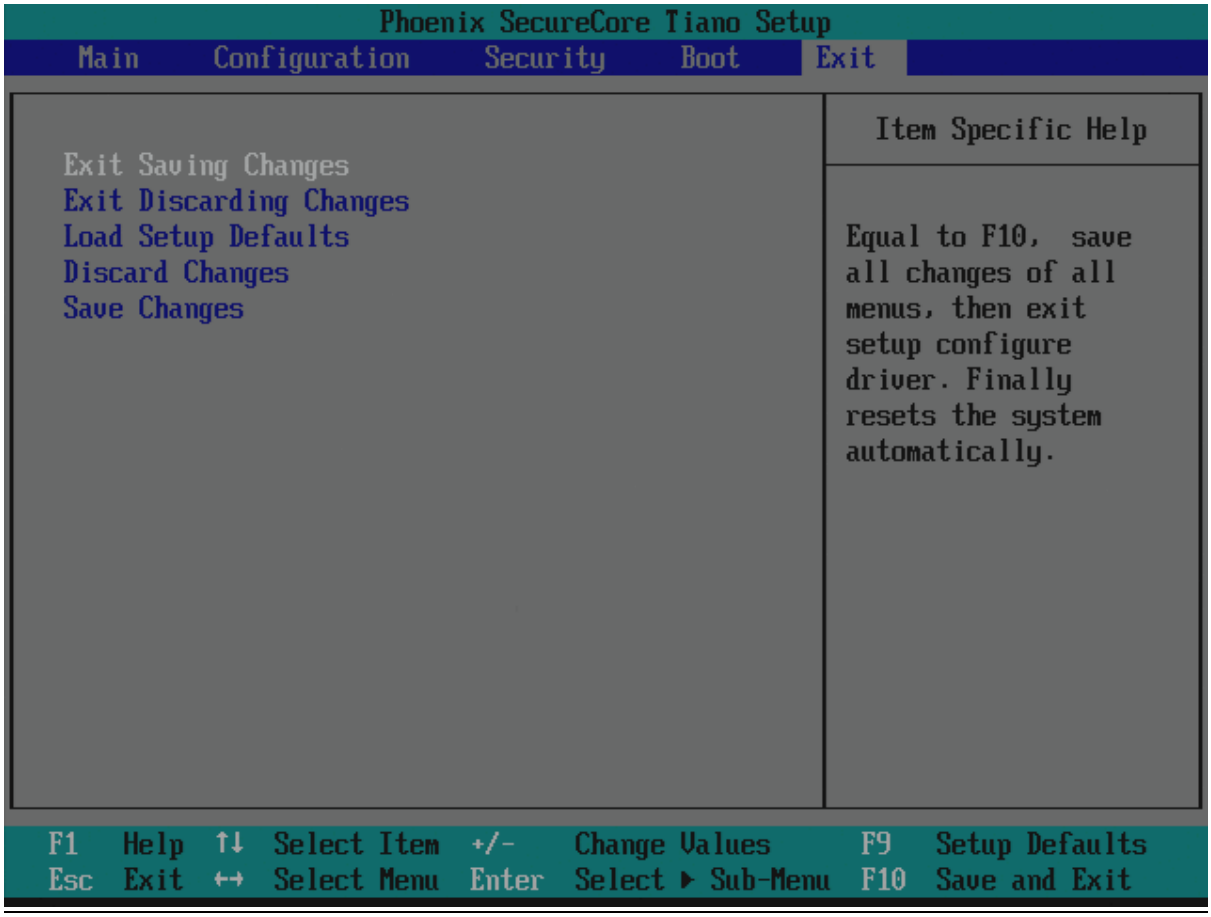
1st Drive

This setting allows users to set the priority of the removable devices. First press <Enter> to enter the sub-menu. Then you may use the arrow keys (↑↓) to select the desired device, then press <+>, <—> or <PageUp>, <PageDown> key to move it up/down in the priority list.

The choice: 1st FLOPPY DRICE, Disabled.

4.6 Exit

This menu allows you to load the BIOS default values or factory default settings into the BIOS and exit the BIOS setup utility with or without changes.



Exit Saving Changes
Equal to F10, save all changes of all menus, then exit setup configure driver. Finally resets the system automatically.

Exit Discarding Changes
Equal to ESC, never save changes, than exit setup configure driver.

Load Setup Defaults
Equal to F9. Load standard default values.

Discard Changes
Load the original value of this boot time. Not the default Setup value.

Save Changes
Save all changes of all menus, but do not reset system. options.

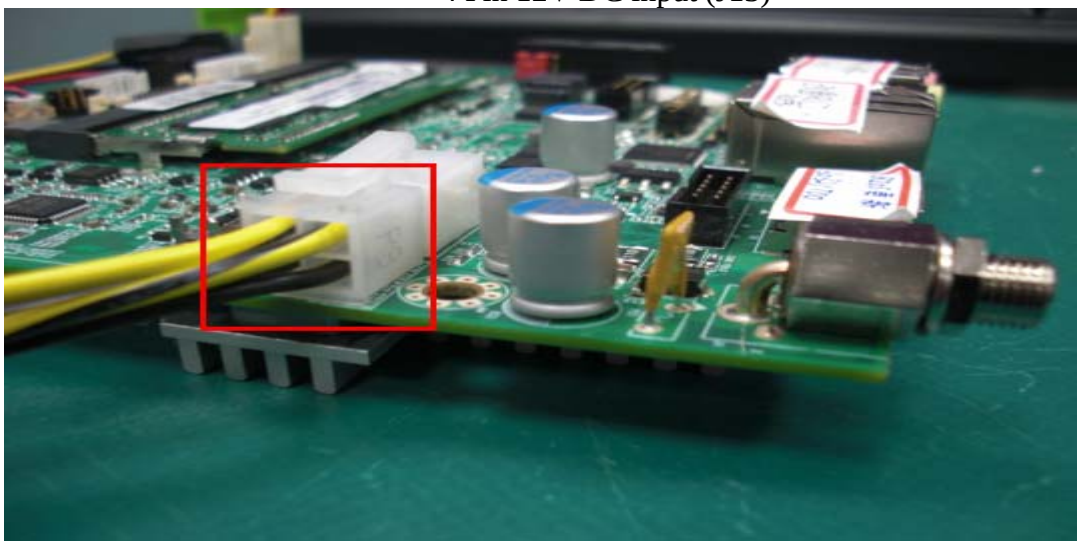
Chapter 5
Troubleshooting

This chapter provides a few useful tips to quickly get NANO-5050 running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will be focusing on system integration issues, in terms of BIOS setting, and OS diagnostics.

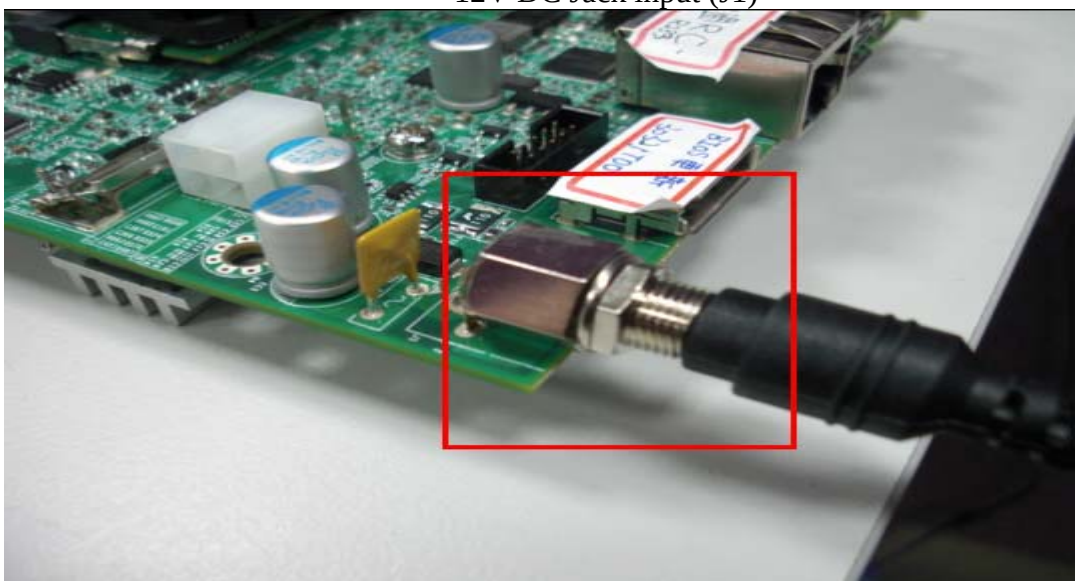
5.1 Hardware Quick Installation

There are two methods to connect the power of NANO-5050 which are 12V DC Jack & 4 Pins 12V DC input. It's able to be chosen either one for NANO-5050. Can be referred as the picture shows blew.

4 Pin 12V DC input (J13)



12V DC Jack input (J1)



※ Please do not connect both power input at the same time!

Please also make sure every other necessary devices are connected before hooking up power source.

Loading the default optimal setting
When prompted with the main setup menu, please scroll down to "Load Setup Defaults", press "Enter" and "Y" to load in default optimal BIOS setup. This will force your BIOS setting back to the initial factory configuration. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting any time when system appears to be unstable in boot up sequence.

5.2 FQA

Question: I forget my password of system BIOS, what am I supposed to do?

Answer: You can simply short 2-3 pins on J14 to clean your password.

Question: I cannot boot up my system!

Answer: Please make sure all the setups were followed the instruction in User's manual. Unplugged any other add-on device to isolate the possibility of external affection and try again. If the SBC still does not boot, please contact with our Technical support department.

Note:
Please visit our technical web site at http://www.portwell.com.tw

For additional technical information, which is not covered in this manual, you can mail to tsd@portwell.com.tw or you can also send mail to our sales, they will be very delighted to forward them to us.

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used for your reference.

System Memory Address Map		
Memory Area	**Size**	**Description**
0000-003F	**1 K**	**Interrupt Area**
0040-004F	**0.3 K**	**BIOS Data Area**
0050-006F	**0.5 K**	**System Data**
0070-0E2E	**54 K**	**DOS**
0E2F-0F6B	**5 K**	**Program Area**
0F6C-9B7F	**560 K**	**【Available】**
9B80-9D7F	**8 K**	**Unused**
First Meg	**-- Conventional memory end at 630K --**	
9D80-9DFF	**2 K**	**Extended BIOS Area**
9E00-9FFF	**8 K**	**Unused**
A000-AFFF	**64 K**	**VGA Graphics**
B000-B7FF	**32 K**	**Unused**
B800-BFFF	**32 K**	**VGA Text**
C000-CF3F	**61 K**	**Video ROM**
CF40-EFFF	**131 K**	**Unused**
F000-FFFF	**64 K**	**System ROM**
HMA	**64 K**	**First 64K Extended**

Interrupt Request Lines (IRQ)

Interrupt Request Lines IRQ		
IRQ#	**Current Use**	**Default Use**
IRQ 0	Unused	System Timer
IRQ 1	System ROM	Keyboard Event
IRQ 2	【Unassigned】	Usable IRQ
IRQ 3	System ROM	COM2
IRQ 4	System ROM	COM1
IRQ 5	【Unassigned】	Usable IRQ
IRQ 6	System ROM	Diskette Event
IRQ 7	Unused	Usable IRQ
IRQ 8	System ROM	Real-Time Clock
IRQ 9	【Unassigned】	Usable IRQ
IRQ 10	【Unassigned】	Usable IRQ
IRQ 11	【Unassigned】	Usable IRQ
IRQ 12	System ROM	IBM Mouse Event
IRQ 13	System ROM	Coprocessor Error
IRQ 14	System ROM	Hard Disk Event
IRQ 15	【Unassigned】	Usable IRQ